

Symphony-Board



CONTENT

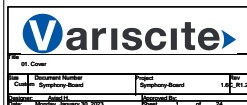
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Disclaimer:

Schematics are for reference only.
Variscite LTD provides no warranty for the use of these schematics.
Schematics are subject to change without notice.

Revision History

Document	Carrier	
1.0	1.0	Initial
1.1	1.1	Released
1.2	1.1	Updated Block Diagrams Added SH1 wire short symbol Updated Compatibility value for SOM pins 68,69,176 Updated SOM pin 22 net name Fixed U22.B1, C113.1 net name Fixed R1-R2,R35-R38 net name
1.3	1.2	Removed SH1 wire short, J1.68 routed to capacitive touch Changed R29 to C185 Changed R123,R127 to N.C. Added resistors R130-132 Removed ADC_INxx alternate function from VAR-SOM-MX8 Symbol Updated PCIe resistor assembly note
1.4	1.2	Updated Parallel Camera/HDMI/DP Note Fixed ETH pin names VAR-SOM-MX8X Symbol
1.5	1.2A	Disconnected R129
1.6	1.2A	Added VAR-SOM-MX8M-MINI Block Diagram and Symbol PRE-RELEASE VERSION!!!! Subject to change without notice
1.7	1.2B	Fixed VAR-SOM-MX8M-MINI Symbol Changed U29,U30,U31 to P/N: PFF2193 Changed R60 to 47K
1.8	1.2C	Update VAR-SOM-MX8M-MINI Symbol to V1.1 with side notes for v1.0B(Early access customers) Update VAR-SOM-MX8M-MINI Block Diagram POR circuitry fed by VCC_SOM: see U7 R60 R61 R40 R60 D5 Removed
1.9	1.2D	Raise VCC_3V3 to Nominal 3.39V for VAR-SOM-MX8M-MINI/NANO power up threshold voltage requirement of >3.35V
1.10	1.2E	Reference for new designs: (changes not implemented in V1.2 BRD) * Added x2 studs for heat plate support * Base_per_3v3 added slew rate limit * U7 (Base POR circuit) added CB_WDOG resistor assembly options * U29 U30 U31 - Added assembly note * VAR-SOM-MX8M-NANO pages added with symbol pinout * VAR-SOM-MX8 Connector update - added NC on /? assembly options * Power switch in OFF position discharge of Custom rails added * Ethernet magnetics - support two Marf: Pulse & UDE; * Base RJ45 LEDs matched to SOM behaviour;
1.11	1.3	* Added VAR-SOM-MX8M-PLUS Preliminary Symbol and Block Diagram Symbol is Pre-Release Version! Subject to change without notice! * All C1210 capacitor footprint updated to C1210_v0 * MS1 to MS6 not assembled
1.12	1.3A	* ETH1 PHY clock filter U9 replaced with 49.5 Ohm /0603 resistor * Added design note for ETH1 switches U8 and U10.
1.13	1.4	* MS5 and MS6 location adopted to heatplate design - Layout * Update J1 Manufacturer P/N, NAME and footprint to represent the assembled part * Replace PCIe AC caps on RX lines with 0 ohm resistors * Updated VAR-SOM-MX8M-PLUS Symbol pins 1 58 80, swap pins 41 43 and 84 147 * J19 Modify Camera connector orientation * Remove U8 U10 analog switches on ETH1 * U9 revert to EMI filter on RGMII_RX clock line * Added RN1 RN2 RN3 R151 R136 isolating stubs on ETH1 RGMII signals * U26 footprint updated to DS * Y1 C68 C67 updated * Support for VAR-SOM-6UL boot: - BOOT_MODE1 - R117 assembled - BOOT_MODE0 - Added PD R149 - USB&A PWR to HOST J23 always enabled * Remove R39 on pin J1-156 to support SOM-MX8MP 2nd MIPI-CSI Lane2 routing * J3 J30 pinout change
1.14	1.4A	* Support for VAR-SOM-MX8MP USB OTG - Changed U5.P4 Pull for board identification, U21.9 connected to GPIO: - Changed R43,R130,R106 to N.C. - Changed R44,R132 to Assembled * Changed Q4 P/N from: TPS27082L (EOL) to -> TPS27081A * Updated VAR-SOM-MX8M-PLUS Block Diagram, Symbol pins 36,38 names * Added notes for SOM pins 29,79,84
1.15	1.4A	Changes in v1.14/1.4A for R43,R44 were not implemented (part of board identification) and only appear in revision history: board identification implemented via EEPROM U3. Board identification required for OS to identify method of OTG ID used: PTN5150 or GPIO
1.16	1.5	* Modified VCC_3V3 to 3.35V nominal for all SOMs. For VAR-SOM-MX8M-MINI/NANO, power up threshold voltage requirement of >3.35V is implemented using Q10,R152 * Added note for VAR-SOM-MX8M-MINI/NANO pin 91
1.17	1.5	* Updated note for I2C#B pull up resistors
1.18	1.5	* Updated note for PTN36043BXY chip
1.19	1.5A	* Q10 changed to 2N7002P.215 Transistor Q10 changed to 2N7002P to stabilize the SOM voltage in the OFF state. Old transistor leakage current (IDG) changed the feedback current and increased the SOM voltage. 2N7002P does not have SG diode that allowed IDSS to flow into the Gate * SOM Pin 84 Note changed
1.20	1.6	Ethernet PHY replaced to ADIN1300 R22,R23,R35,R36 assembled with Ferrite Bead C185 assembled with 10K resistor, R30 not assembled U2 changed to CBTL02043B USB3 crossover switch changed to CBTL02043B
1.21	1.6A	Due to EOL: U35 changed to NFL18ZT207H1A3D Due to allocation problems: U13 changed to SN65HVD232QDR
1.22	1.6B	Due to allocation problems: U22,U29,U30,U31 changed to P/N: PFF2194
1.23	1.6C	Added VAR-SOM-AM62 Block Diagram and Symbol Added VAR-SOM-MX93 Block Diagram and Symbol Temporary removed compatibility notes Added hand wired EXP_MDIO_EN line.



03.SOM

For cross probing between SOM symbol and the specific SOM Connector used, set the "Implementation" property value in SOM port symbol to one of the following:

1. VAR-SOM-MX6
2. VAR-SOM-MX8
3. VAR-SOM-MX8X
4. VAR-SOM-MX8M-MINI
5. VAR-SOM-MX8M-NANO
6. VAR-SOM-MX8M-PLUS
7. VAR-SOM-MX93
8. VAR-SOM-AM62

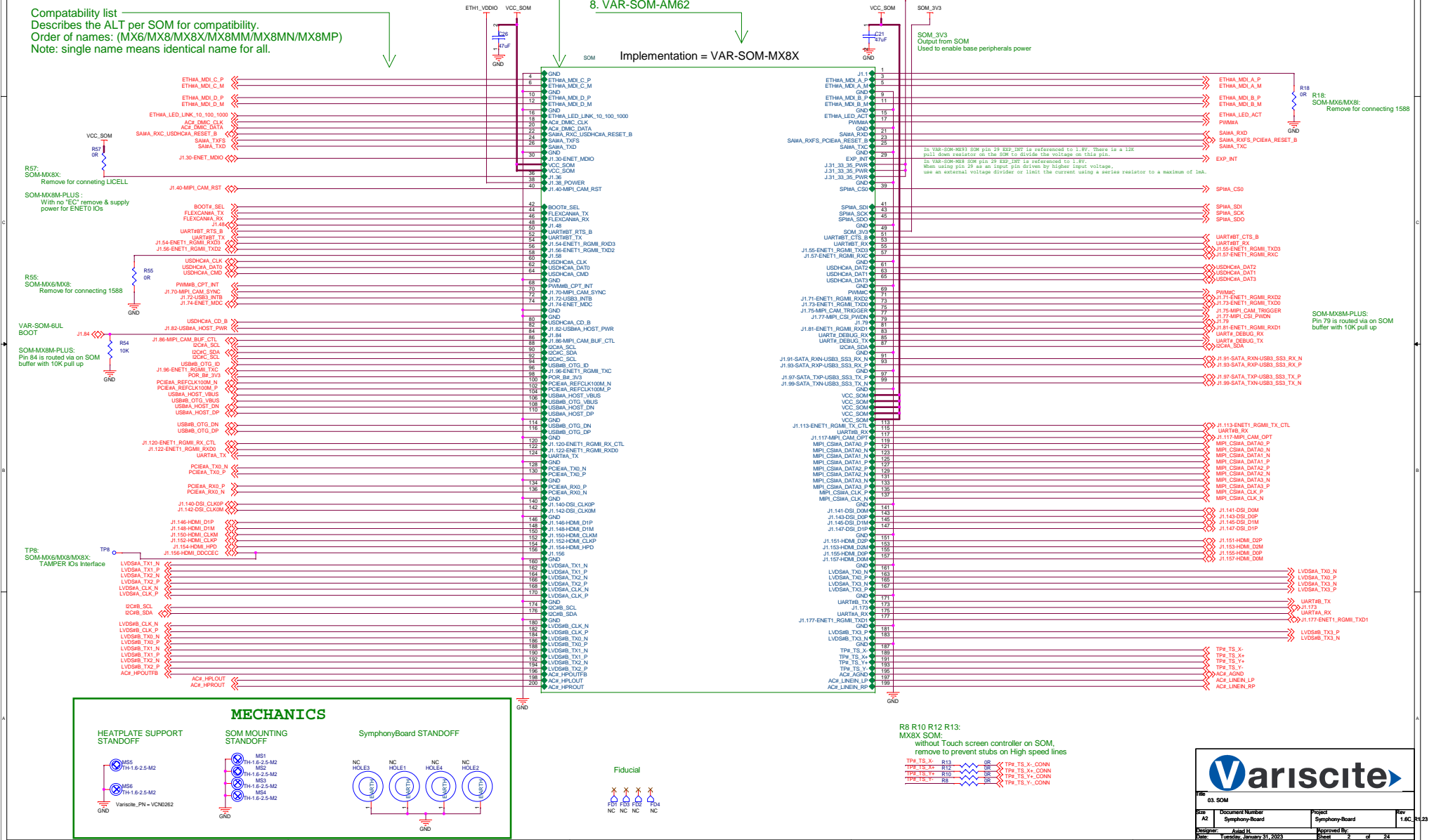
For complete alternate function per pin and specific SOM:
please refer to "VAR-SOMs Compatibility and Pinout.XLS" located at:
ftp://ftp.variscite.com/SOM_Compatibility

OFF PAGE CONNECTOR INDEX:

1. Function# : Interface common to ALL SOMs
2. J1.xxx-Function : Interface common to certain SOMs or Used for carrier board common function
3. J1.xxx : No common interface

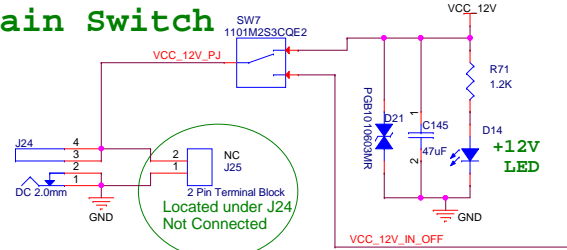
Compatibility list

Describes the ALT per SOM for compatibility.
Order of names: (MX6/MX8/MX8X/MX8MM/MX8MN/MX8MP)
Note: single name means identical name for all.

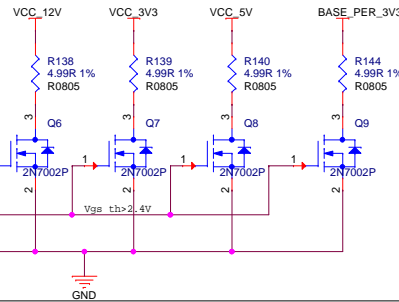


05. Power, Reset, Boot, RTC, EEPROM

12VDC INPUT Main Switch



POWER DISCHARGE



SOM BOOTSTRP

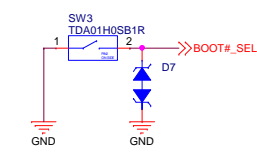
Boot Options:

OFF : INT

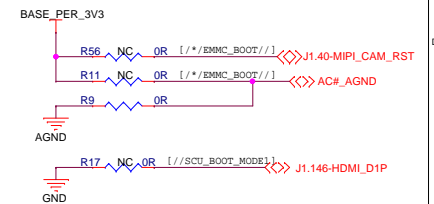
ON : SD

Internal boot is from eMMC

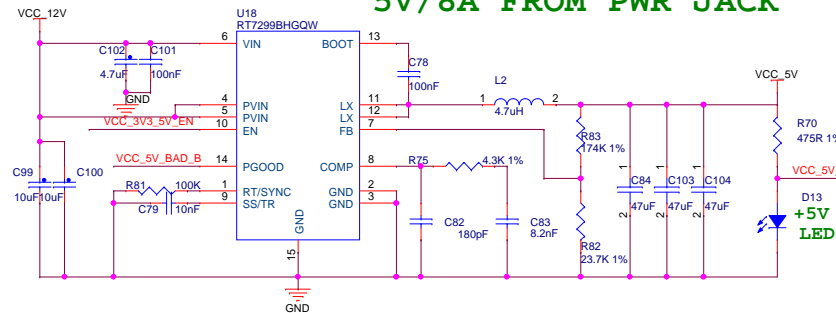
MX6 for eMMC boot see additional changes note



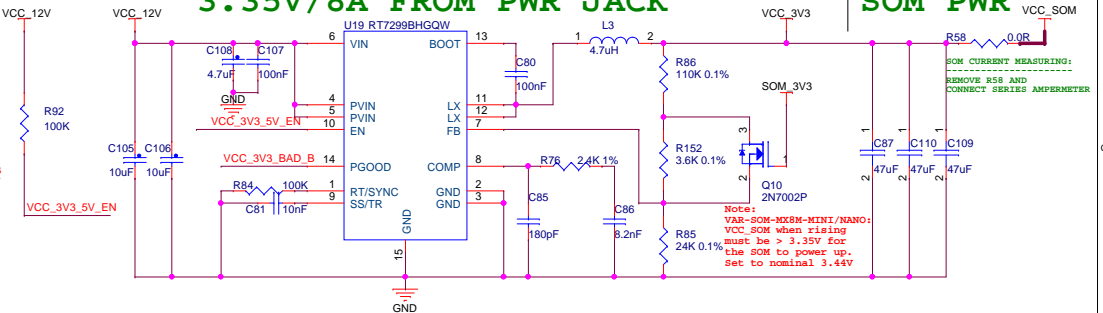
For supporting MX6 eMMC boot option:
Remove R9
Assemble R56,R11
Note: Normal configuration is with NAND



5V/8A FROM PWR JACK

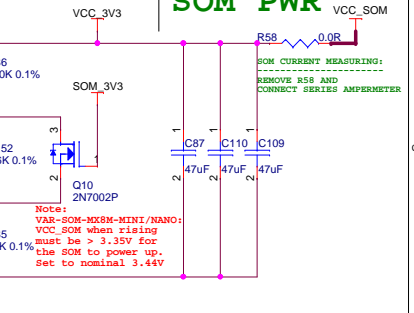


3.35V/8A FROM PWR JACK

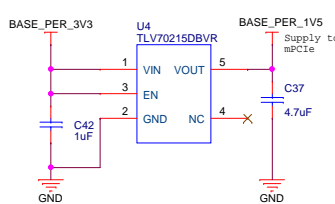


SOM PWR

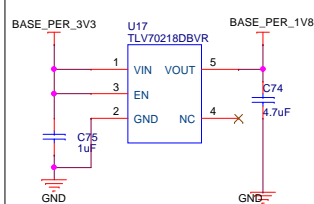
SOM CURRENT MEASURING:
REMOVE R58 AND
CONNECT SERIES AMPERMETER



1.5V BASE

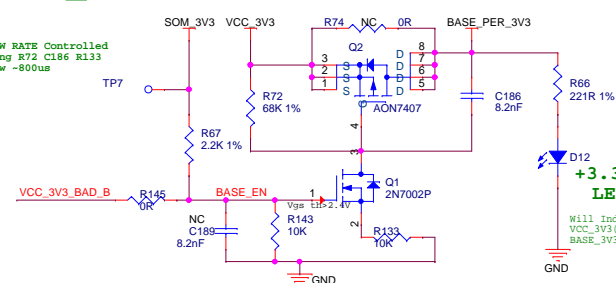


1.8V BASE

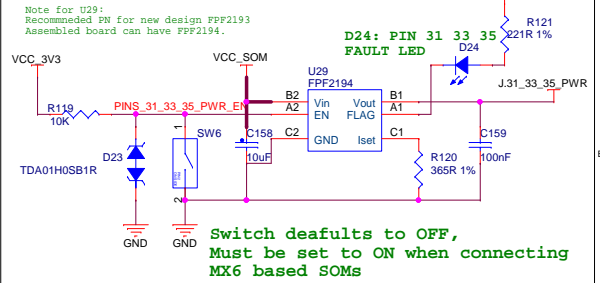


BASE_3V3

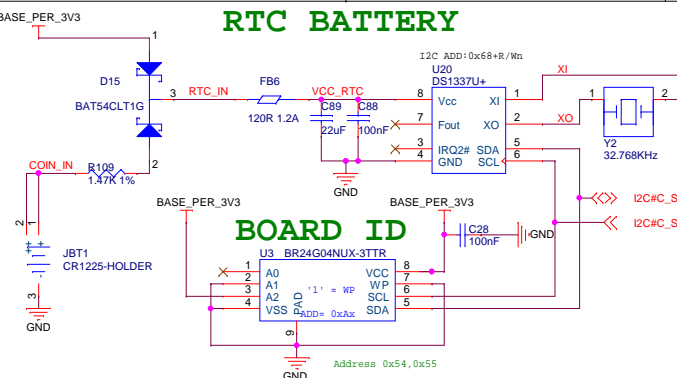
SLEW RATE Controlled
Using R72 C186 R133
slew ~800us



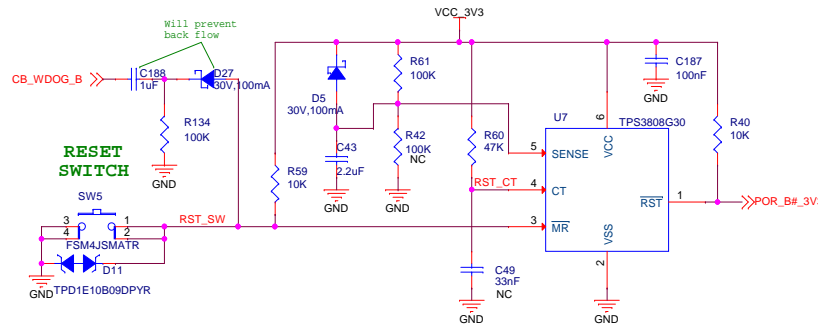
PINS 31 33 35 POWER



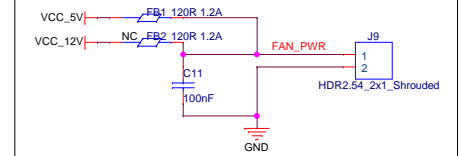
RTC BATTERY



RESET CIRCUITRY



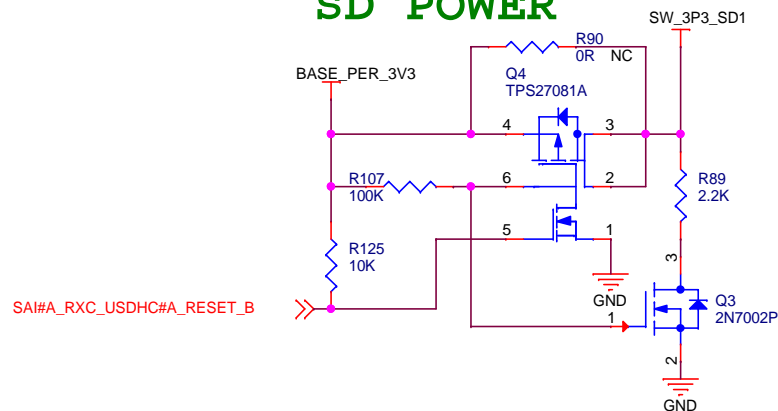
FAN PWR



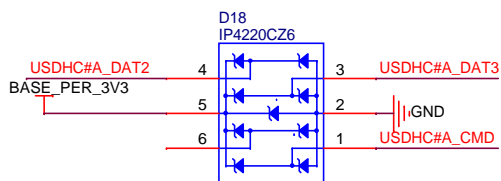
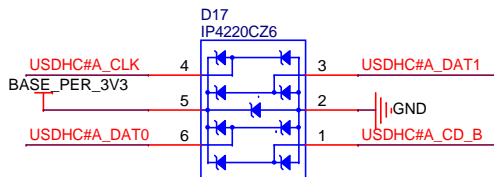
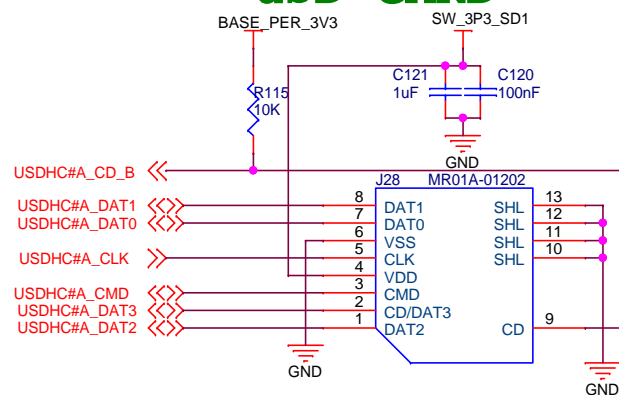
Title 05. Power,Reset,Boot,RTC,EEPROM			
Size A3	Document Number	Project	Rev 1.6C_R1.23
Designer Aviad H.	Approved By:		
Date Monday, January 30, 2023	Sheet 3	of 24	

06. uSD, Audio,CAN

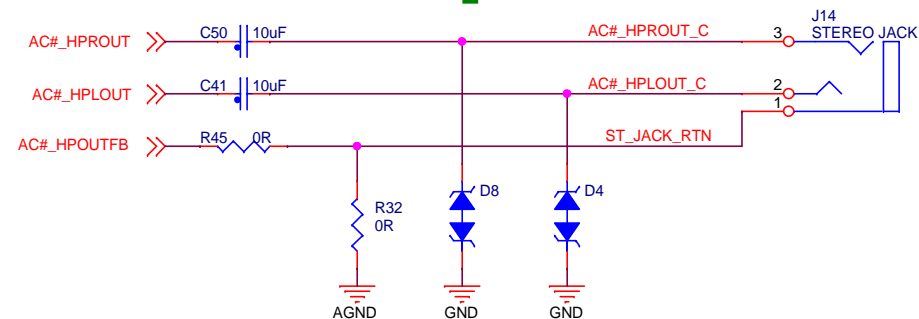
SD POWER



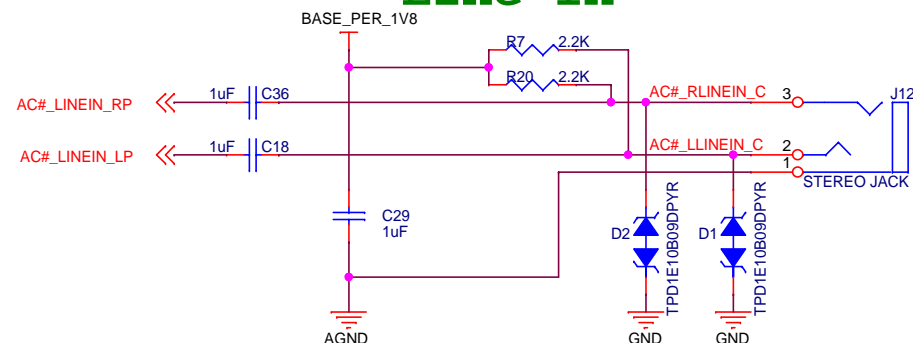
uSD CARD



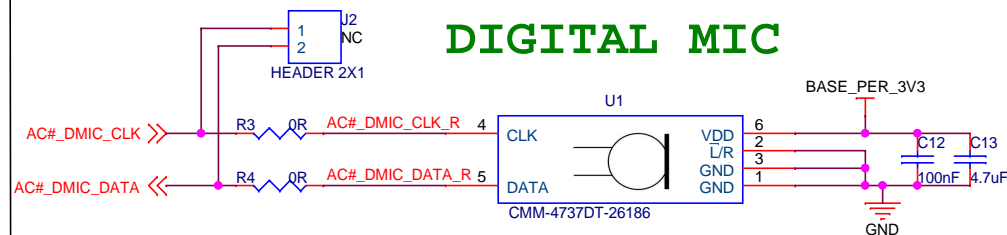
Headphones



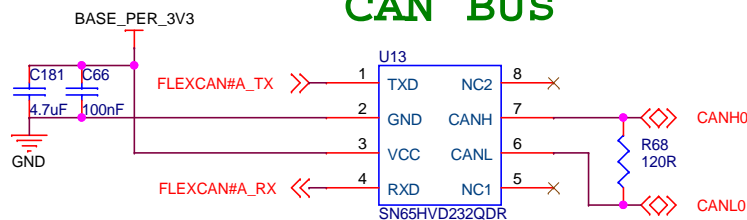
Line In



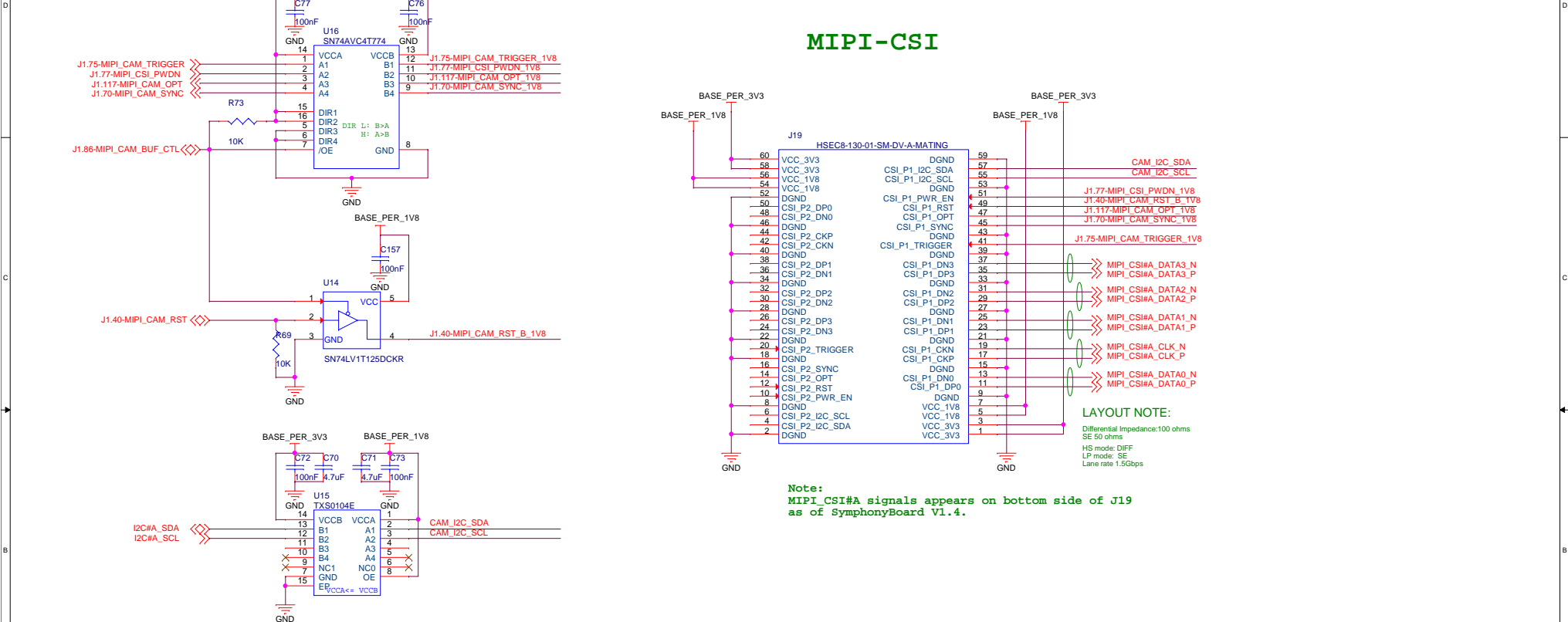
DIGITAL MIC



CAN BUS



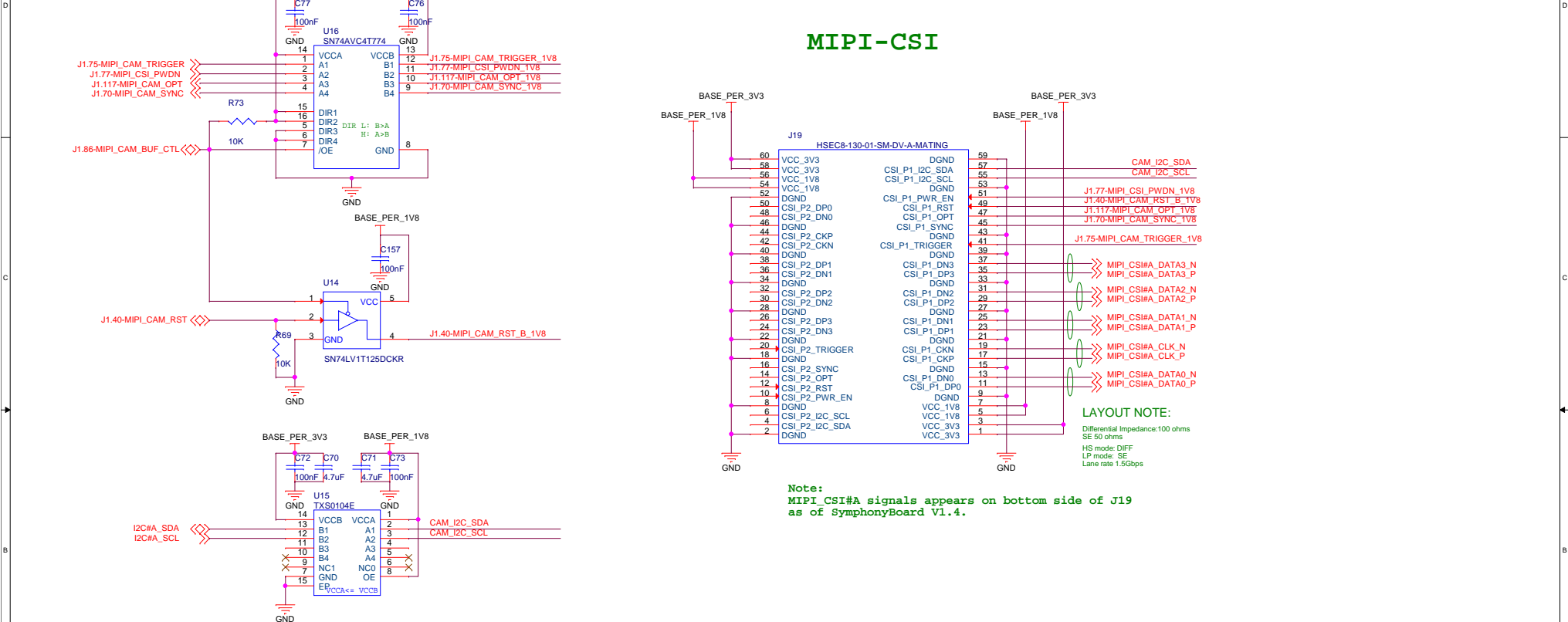
Title 06. uSD, Audio,CAN			
Size A4	Document Number Symphony-Board	Project Symphony-Board	Rev 1.6C R1.2
Designer: Monday, January 30, 2023		Approved By: Sheet 4 of 24	



MIPI-CSI

Note:
 MIPI_CSI#A signals appears on bottom side of J19
 as of SymphonyBoard V1.4.

LAYOUT NOTE:
 Differential Impedance: 100 ohms
 SE 50 ohms
 HS mode: DIFF
 LP mode: SE
 Lane rate 1.5Gbps



MIPI-CSI

Note:
MIPI_CSI#A signals appears on bottom side of J19
as of SymphonyBoard V1.4.

LAYOUT NOTE:
Differential Impedance: 100 ohms
SE 50 ohms
HS mode: DIFF
LP mode: SE
Lane rate 1.5Gbps

Note for U32 (analog switch):
Switch is capable support for the following adapters:

J13: MX6/MX8-HDMI, MX8-DP, MX8X-CSI, MX8MP-2nd MIPI-CSI

Note for U32 (analog switch):
Switch is capable support for the following adapters:

J13: MX6/MX8-HDMI, MX8-DP, MX8X-CSI, MX8MP-2nd MIPI-CSI

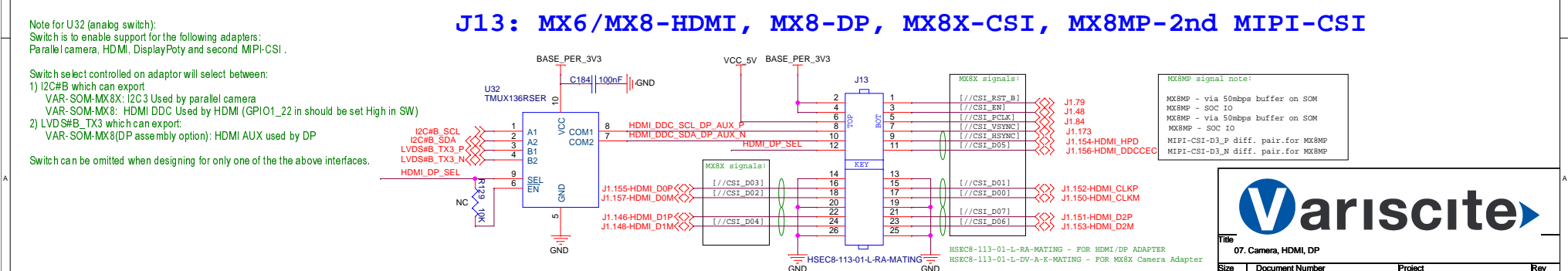
Note for U32 (analog switch):
Switch is in enable position for the following adapters:

J13: MX6/MX8-HDMI, MX8-DP, MX8X-CSI, MX8MP-2nd MIPI-CSI

- Note for U32 (analog switch):
Switch is in enable position for the following adapters:
- J13: MX6/MX8-HDMI, MX8-DP, MX8X-CSI, MX8MP-2nd MIPI-CSI**

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J13: MX6/MX8-HDMI, MX8-DP, MX8X-CSI, MX8MP-2nd MIPI-CSI

Note for U32 (analog switch):
Switch is to enable support for the following adapters:
Parallel camera, HDMI, DisplayPort and second MIPI-CSI.

Switch select controlled on adaptor will select between:
1) I2C#B which can export
VAR-SOM-MX8X: I2C3 Used by parallel camera
VAR-SOM-MX8: HDMI DDC Used by HDMI (GPIO1_22 in should be set High in SW)
2) LVD#B_TX3 which can export:
VAR-SOM-MX8(DP assembly option): HDMI AUX used by DP

Switch can be omitted when designing for only one of the the above interfaces.

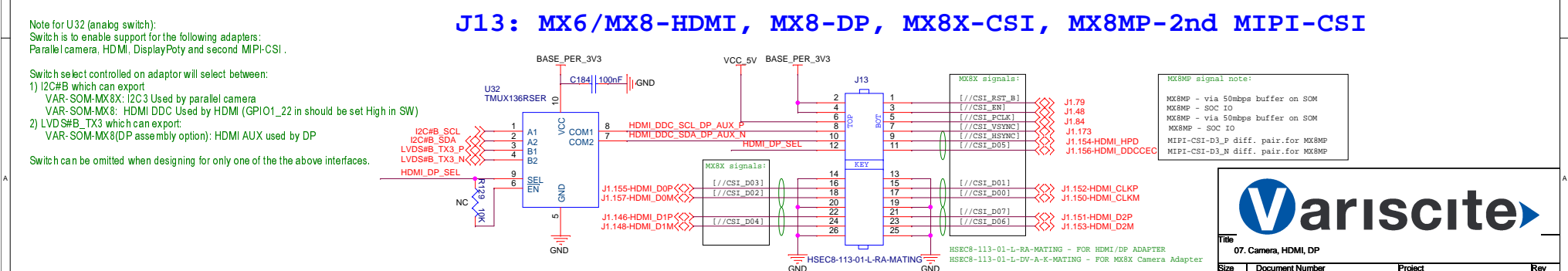
MX8MP signal note:
MX8MP - via 50Mbps buffer on SOM
MX8MP - SOC IO
MX8MP - via 50Mbps buffer on SOM
MX8MP - SOC IO
MIPI-CSI-D3_P diff. pair.for MX8MP
MIPI-CSI-D3_N diff. pair.for MX8MP

MX8X signals:
[[/CSI_RST_B]] J1.79
[[/CSI_EN]] J1.48
[[/CSI_PCLK]] J1.84
[[/CSI_VSYNC]] J1.173
[[/CSI_BSYN]] J1.154-HDMI_HPD
[[/CSI_D05]] J1.156-HDMI_DDCCEC

MX8X signals:
[[/CSI_D03]] J1.155-HDMI_D0P
[[/CSI_D02]] J1.157-HDMI_D0M
[[/CSI_D04]] J1.146-HDMI_D1P
[[/CSI_D04]] J1.148-HDMI_D1M

MX8X signals:
[[/CSI_D01]] J1.152-HDMI_CLKP
[[/CSI_D00]] J1.150-HDMI_CLKM
[[/CSI_D07]] J1.151-HDMI_D2P
[[/CSI_D06]] J1.153-HDMI_D2M

HSECB-113-01-L-RA-MATING - FOR HDMI/DP ADAPTER
HSECB-113-01-L-DV-A-K-MATING - FOR MX8X Camera Adapter



J13: MX6/MX8-HDMI, MX8-DP, MX8X-CSI, MX8MP-2nd MIPI-CSI

Note for U32 (analog switch):
Switch is to enable support for the following adapters:
Parallel camera, HDMI, DisplayPort and second MIPI-CSI.

Switch select controlled on adaptor will select between:
1) I2C#B which can export
VAR-SOM-MX8X: I2C3 Used by parallel camera
VAR-SOM-MX8: HDMI DDC Used by HDMI (GPIO1_22 in should be set High in SW)
2) LVD#B_TX3 which can export:
VAR-SOM-MX8(DP assembly option): HDMI AUX used by DP

Switch can be omitted when designing for only one of the the above interfaces.

MX8MP signal note:
MX8MP - via 50Mbps buffer on SOM
MX8MP - SOC IO
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MX8MP - SOC IO
MIPI-CSI-D3_P diff. pair.for MX8MP
MIPI-CSI-D3_N diff. pair.for MX8MP

MX8X signals:
[[/CSI_RST_B]] J1.79
[[/CSI_EN]] J1.48
[[/CSI_PCLK]] J1.84
[[/CSI_VSYNC]] J1.173
[[/CSI_BSYN]] J1.154-HDMI_HPD
[[/CSI_D05]] J1.156-HDMI_DDCCEC

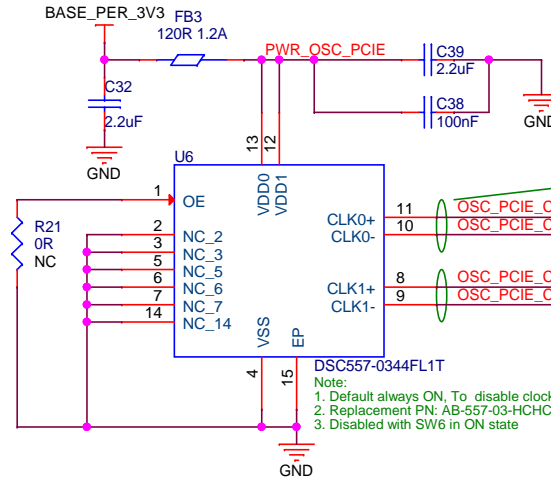
MX8X signals:
[[/CSI_D03]] J1.155-HDMI_D0P
[[/CSI_D02]] J1.157-HDMI_D0M
[[/CSI_D04]] J1.146-HDMI_D1P
[[/CSI_D04]] J1.148-HDMI_D1M

MX8X signals:
[[/CSI_D01]] J1.152-HDMI_CLKP
[[/CSI_D00]] J1.150-HDMI_CLKM
[[/CSI_D07]] J1.151-HDMI_D2P
[[/CSI_D06]] J1.153-HDMI_D2M

HSECB-113-01-L-RA-MATING - FOR HDMI/DP ADAPTER
HSECB-113-01-L-DV-A-K-MATING - FOR MX8X Camera Adapter

09. PCIe

PCIe CLK



LAYOUT NOTE:

Differential Impedance:
100 ohms

PCIE#A_REFCLK100M_P
PCIE#A_REFCLK100M_N

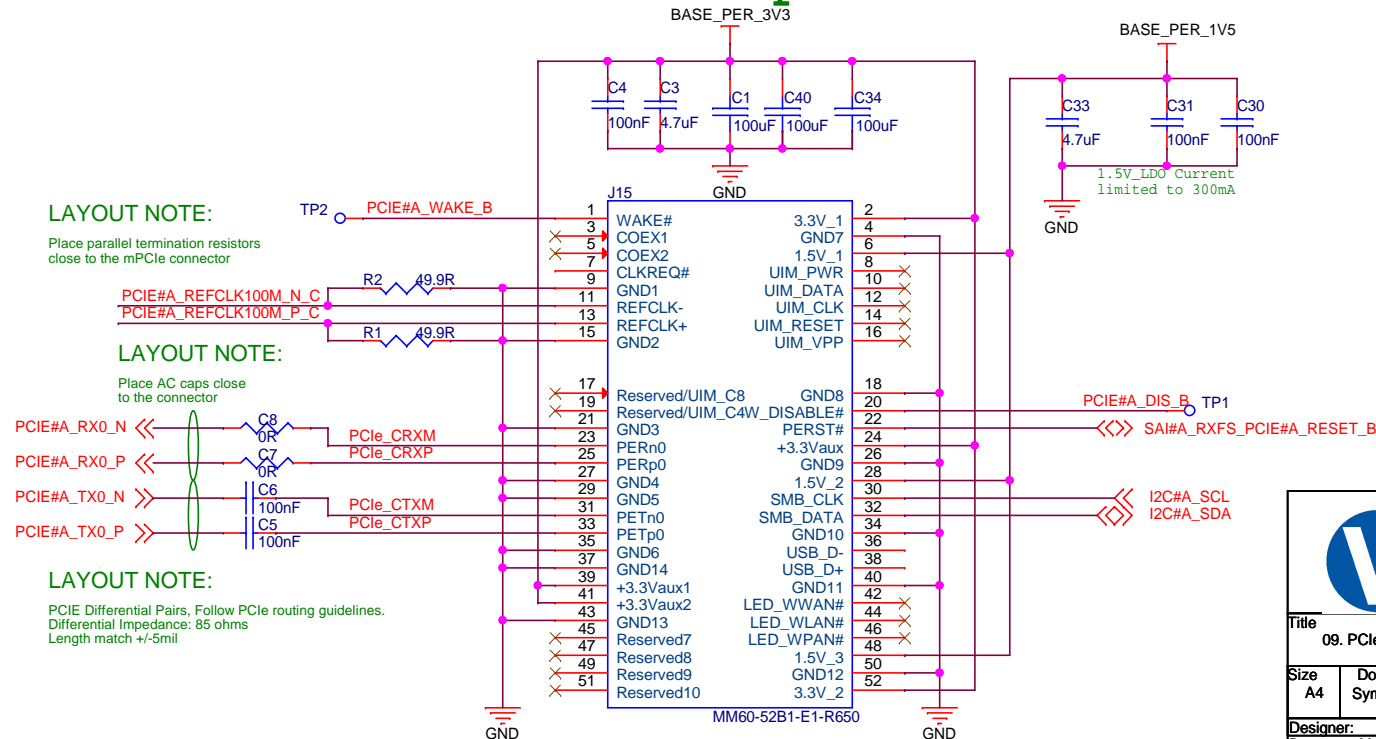
SOM-6UL NAND
signals should
not be driven

PCIE#A_REFCLK100M_P_C
PCIE#A_REFCLK100M_N_C

LAYOUT NOTE:

Place parallel termination resistors
as close to the SOM connector
as possible.

mPCIexp



LAYOUT NOTE:

Place parallel termination resistors
close to the mPCIe connector

LAYOUT NOTE:

Place AC caps close
to the connector

LAYOUT NOTE:

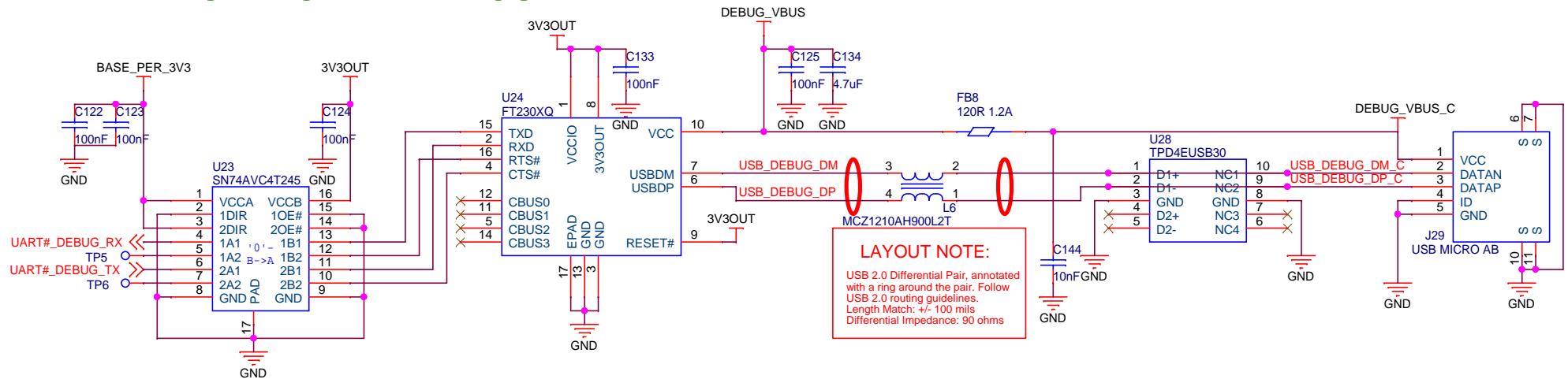
PCIe Differential Pairs, Follow PCIe routing guidelines.
Differential Impedance: 85 ohms
Length match +/-5mil



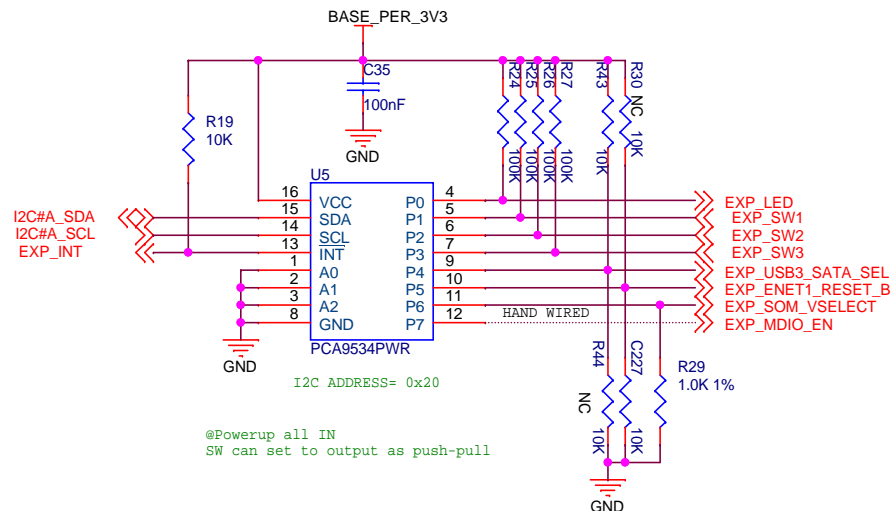
Title 09. PCIe			
Size A4	Document Number Symphony-Board	Project	Rev 1.6C_R1.23
Designer: Date: Monday, January 30, 2023		Approved By: Sheet 7 of 24	

10. Debug, GPIO Exp, Buttons, LED

USB UART DEBUG

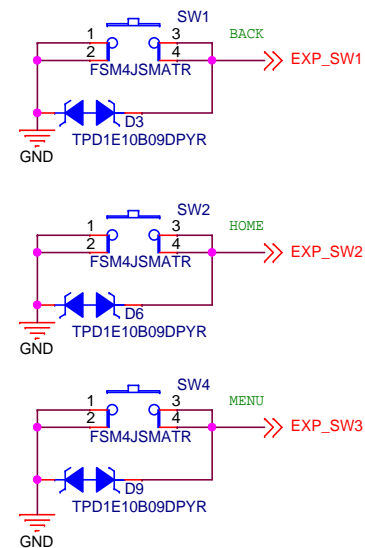


GPIO EXPANDER



In VAR-SOM-MX8 SOM pin 29 EXP_INT is referenced to 1.8V.
When using pin 29 as an input pin driven by higher input voltage,
use an external voltage divider or limit the current using a series resistor to a maximum of 1mA.

GP BUTTON



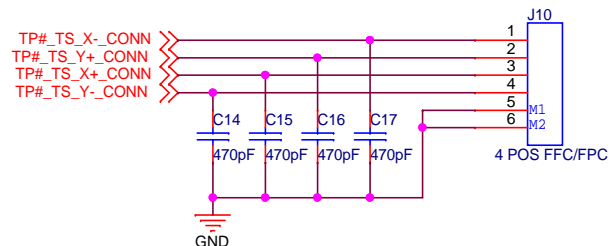
GP LED



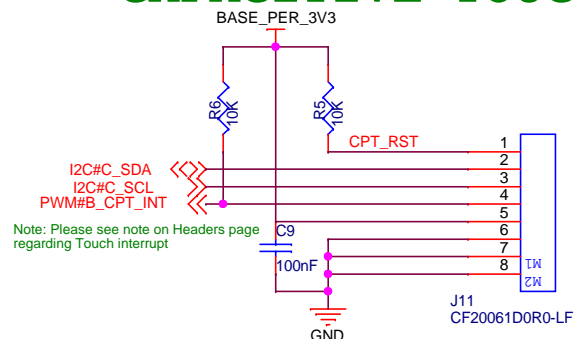
Title 10. Debug, GPIO Exp, Buttons, LED			
Size A4	Document Number Symphony-Board	Project	Rev 1.6C_R1.23
Designer: Aviad H.		Approved By:	
Date: Monday, January 30, 2023		Sheet 8 of 24	

11. LVDS, DSI, Touch

RESISTIVE TOUCH



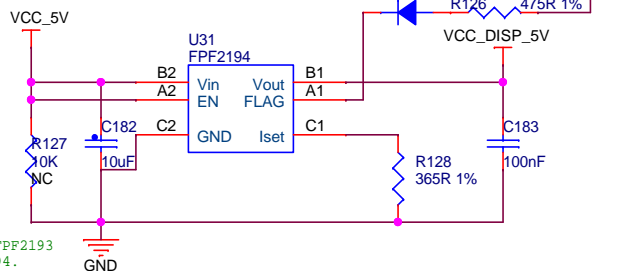
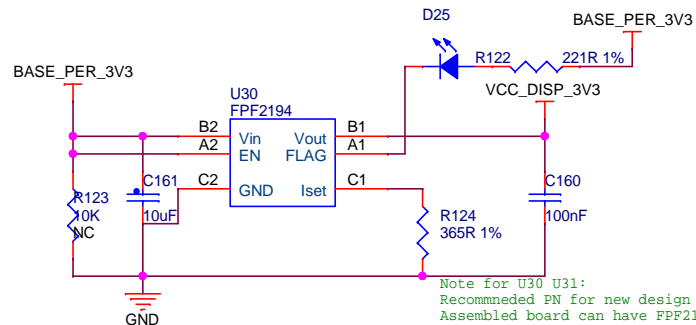
CAPACITIVE TOUCH



See note in :
"Headers" Page 14

J1.57_EXT <<>
CB_WDOG_B >>
J1.82-USB#A_HOST_PWR >>
CB-USB#A_HOST_PWR >>

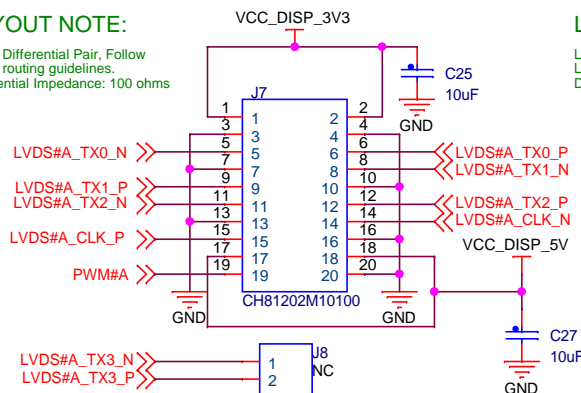
Short circuit protection



LVDS DISPLAY A

LAYOUT NOTE:

LVDS Differential Pair, Follow
LVDS routing guidelines.
Differential Impedance: 100 ohms

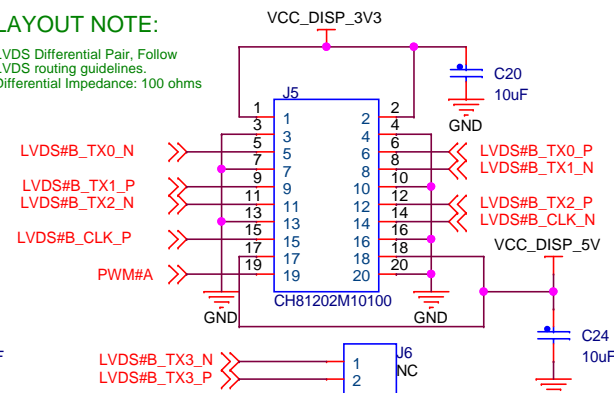


Note: It is recommended to add placeholders
for common mode chokes/ferrites on the LVDS lines
for improvement of EMI suppression

LVDS DISPLAY B

LAYOUT NOTE:

LVDS Differential Pair, Follow
LVDS routing guidelines.
Differential Impedance: 100 ohms

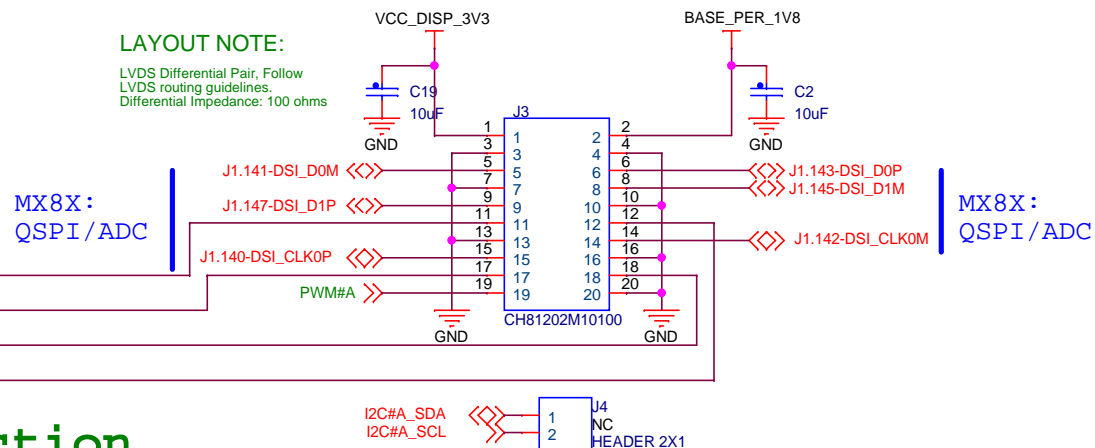


Note: It is recommended to add placeholders
for common mode chokes/ferrites on the LVDS lines
for improvement of EMI suppression

MIPI DSI DISPLAY

LAYOUT NOTE:

LVDS Differential Pair, Follow
LVDS routing guidelines.
Differential Impedance: 100 ohms



Title 11. LVDS, DSI, Touch			
Size A4	Document Number Symphony-Board	Project Symphony-Board	Rev 1.6C R1.2
Designer: Monday, January 30, 2023		Approved By: Sheet 9 of 24	

A vertical number line with four points labeled A, B, C, and D from bottom to top. A horizontal arrow points from point C to point B.

C



A

1





Variscite



Title

12. USB Host

Size	Document Number	Project	Rev
A4	Symphony-Board	Symphony-Board	1.6C

Designer: Aviad H.

Date: Monday, January 30, 2023

Approved By:

Sheet 10 of 24

A vertical bar is divided into four segments labeled A, B, C, and D from bottom to top. An arrow points to the boundary between segments B and C.

R1.2

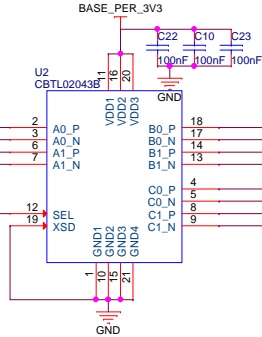
13. USB3, uSATA

SATA/USB select

J1.93-SATA_RXP-USB3_SS3_RX_P
J1.91-SATA_RXN-USB3_SS3_RX_N
J1.97-SATA_TXP-USB3_SS3_TX_P
J1.99-SATA_TXN-USB3_SS3_TX_N

EXP_USB3_SATA_SEL

SEL = LOW: A <-> B
SEL = HIGH: A <-> C
XSD = LOW: ON
XSD = HIGH: OFF
By default, lines routed to SATA



LAYOUT NOTE:

USB 3.0 Differential Pair, annotated with a ring around the pair. Follow USB 3.0 routing guidelines. Differential Impedance: 90 ohms

USB3_SS3_RX_P
USB3_SS3_RX_N
USB3_SS3_TX_P
USB3_SS3_TX_N
SATA_RXP
SATA_RXN
SATA_TXP
SATA_TXN

LAYOUT NOTE:

SATA Differential Pair, Follow SATA routing guidelines. Differential Impedance: 85 ohms Length match +/-5mil

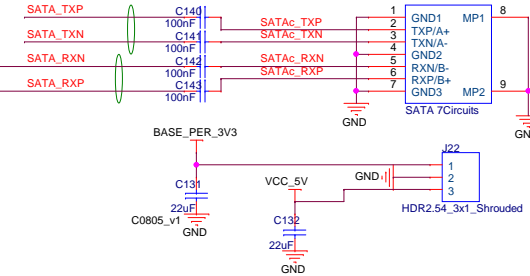
SATA 2.0

LAYOUT NOTE:

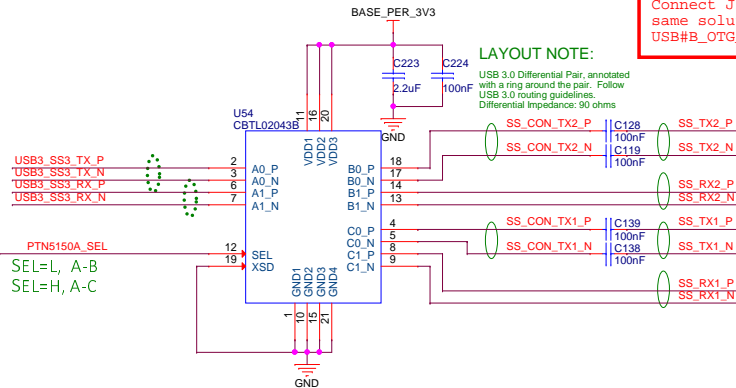
SATA Differential Pair, Follow SATA routing guidelines. Differential Impedance: 85 ohms Length match +/-5mil

LAYOUT NOTE:

Layout Note Place AC caps close to the connector



USB TYPE C Circuitry



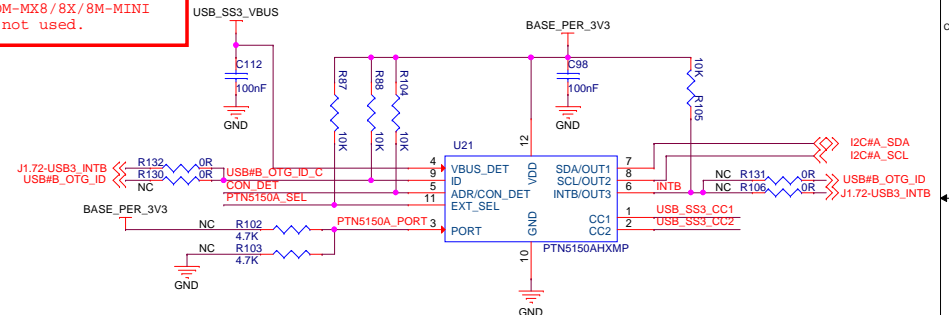
LAYOUT NOTE:

USB 3.0 Differential Pair, annotated with a ring around the pair. Follow USB 3.0 routing guidelines. Differential Impedance: 90 ohms

SS_CON_TX2_P
SS_CON_TX2_N
SS_TX2_P
SS_TX2_N
SS_TX1_P
SS_TX1_N
SS_RX1_P
SS_RX1_N

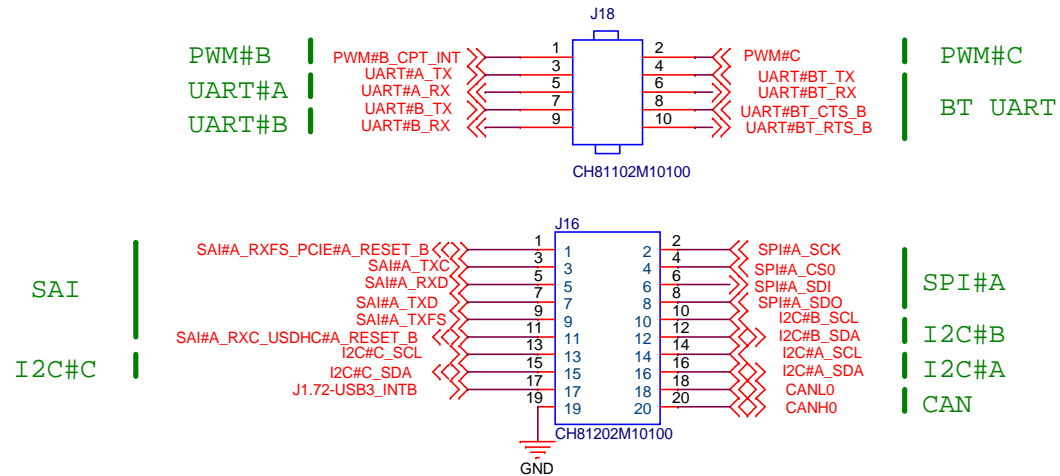
Usage of native USB_ID for iMX8MP requires patches not included in the formal release, pull up should be to 1.8V.
For simple OTG function for VAR-SOM-MX8M-PLUS Connect J1.72 GPIO to U22 PTN ID output - same solution applies also for VAR-SOM-MX8/8X/8M-MINI USB#B_OTG_ID can be left floating if not used.

Config Channel Logic Detection & Indication of Plug Orientation

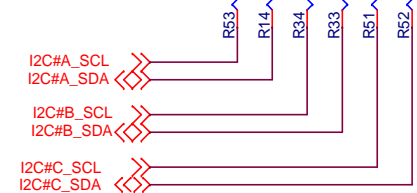


14. Headers

Headers arranged for compatible alternate function

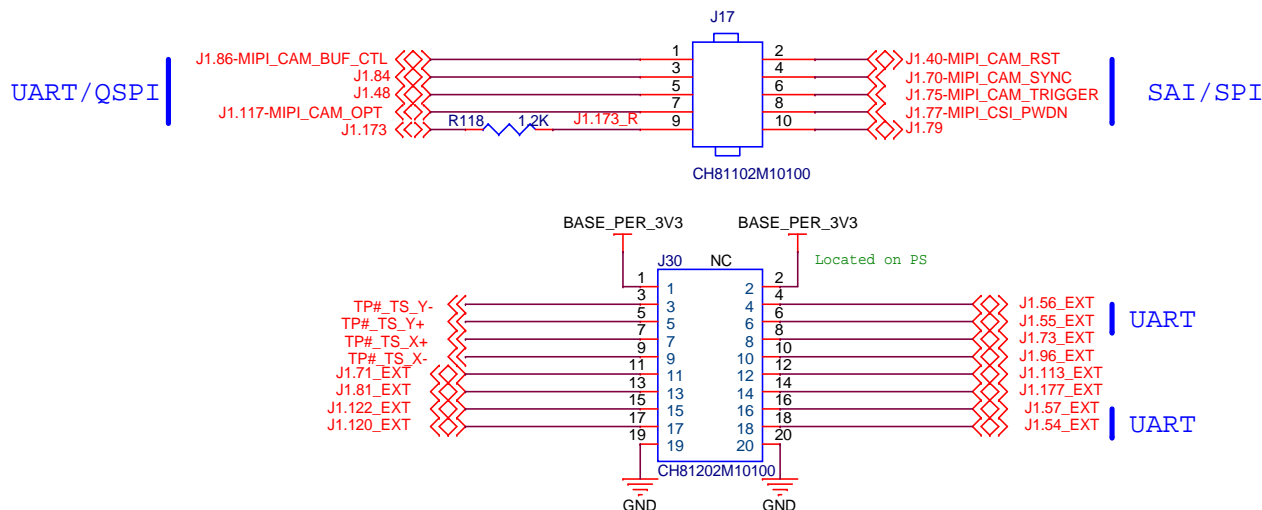


I2C PULL UPS



I2C_A has internal pulls in Camera buffer
I2C_B has internal pulls in MX6/MX8/MX8X/MX8MP SOMs.
For MX8MM/MX8MN/6UL SOMs - external pull ups should be added.

Headers arranged for partial compatible alternate function



COLD RESET ON WDOG_B EVENT for MX6/SOLO and 6UL SOMs

Listed above SOMs require short on headers to get "reboot" to function.
For all other watch dog looped on SOM

CB_WDOG_B	>> Symphony Board reset circuitry watch dog input	See J3.17
J1.57_EXT	<< SOM_6UL: PIN57 WDOG1_B	See J3.11
PWM#B_CPT_INT	<< MX6/SOLO: PIN68 WDOG1_B	See J18.1

USB#A Host VBUS power control

In order to control the USB#A HOST VBUS power a short is required:		
CB-USB#A_HOST_PWR	>> Symphony Board U22 control input	See J3.12
J1.82-USB#A_HOST_PWR	>>	See J3.18

For complete header alternate function refer to "VAR-SOMs_Compatibility_and_Pinout.XLS" located at:
ftp://ftp.variscite.com/SOM_Compatibility



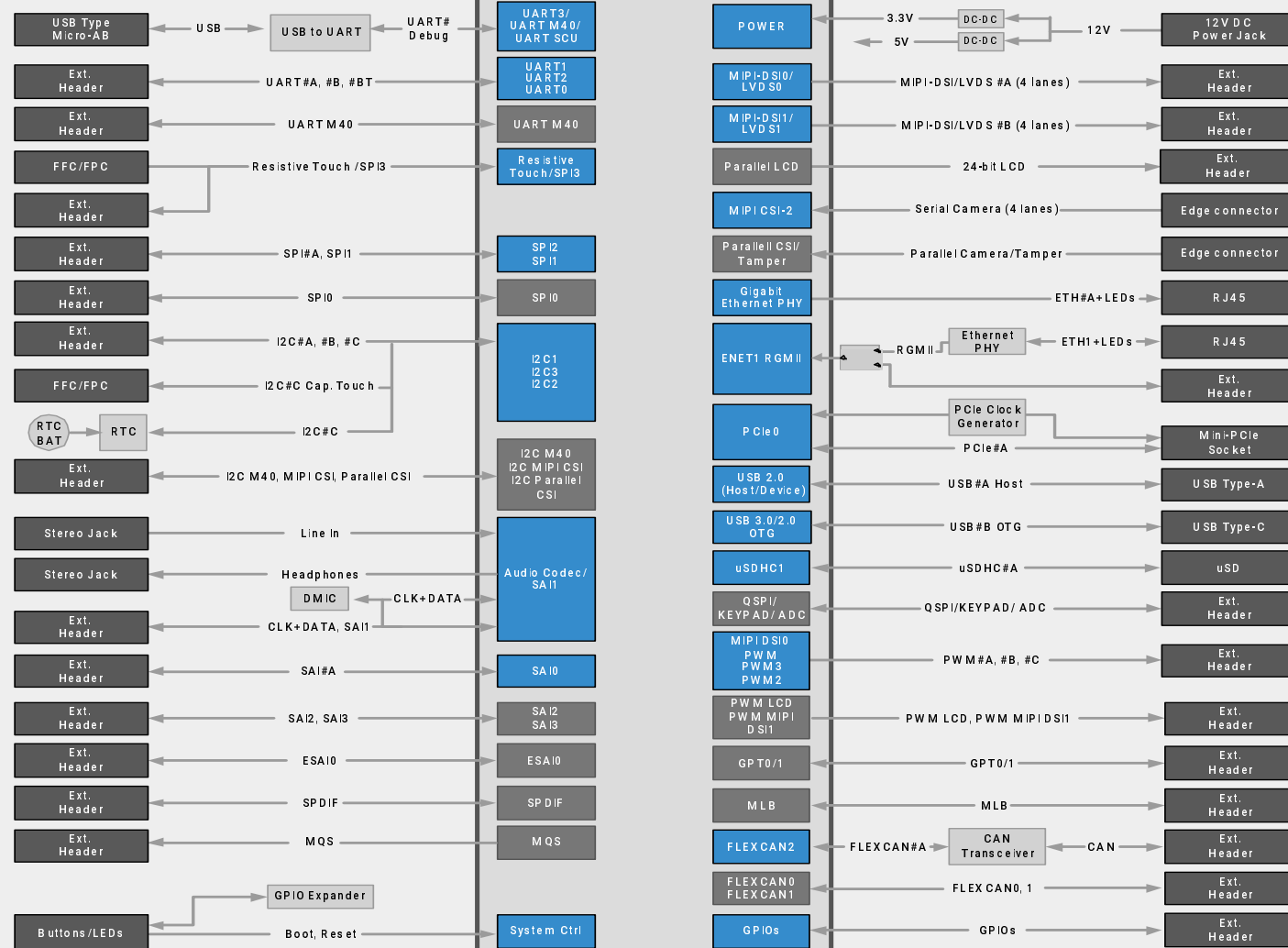
Title 14. Headers			
Size A4	Document Number Symphony-Board	Project Symphony-Board	Rev 1.6C R1.2
Designer: Monday, January 30, 2023		Approved By: Sheet 12 of 24	

02. Block Diagram VAR-SOM-MX8X

Symphony-Board

Doc rev 1.1

VAR-SOM-MX8X



Pin2pin with additional VAR-SOM products.
Please check pinlist document for details

Not Compatible



Title
02. Block Diagram VAR-SOM-MX8X

Size	Document Number	Project	Rev
A3	Symphony-Board	Symphony-Board	1.6C, R1.23
Designer:	Aviad H.	Approved By:	
Date:	Monday, January 30, 2023	Sheet	23 of 24

04. VAR-SOM-MX8X Connector

