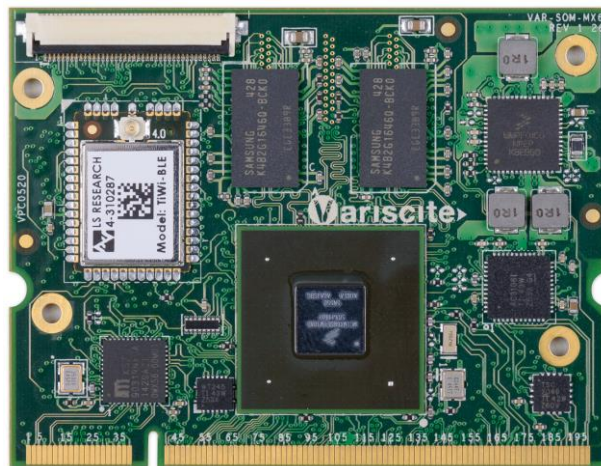




VARISCITE LTD.

VAR-SOM-MX6 v1.1/v1.2x Datasheet

Freescale i.MX6™ - based System-on-Module



VARISCITE LTD.

VAR-SOM-MX6 Datasheet

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| Revision | Date | Notes |
|----------|------------|--|
| 1.0 | 29/7/2012 | Initial |
| 1.01 | 2/12/2012 | Block Diagram update CSI0 pins description on table 3.1 update |
| 1.1 | 6/2/2013 | Datasheet general update. |
| 1.16 | 29/3/2013 | Section 6.3: Dual core current draw typo fixed. |
| 1.17 | 3/5/2013 | UART5 signals pin number typo fixed |
| 1.18 | 27/5/2013 | Section 4.3.2 fixed |
| 1.19 | 3/7/2013 | CSI0 pins description in section 4.3.2 |
| 1.20 | 18/7/2013 | CSI1 CSI0 pins description in section 4.3.2 |
| 1.21 | 20/7/2013 | Section 4.19.1 Boot select configuration description |
| 1.22 | 29/7/2013 | Pin 56 clarification in mux table |
| 1.23 | 29/7/2013 | Section 3.2 pins 52,54,56 |
| 1.24 | 11/9/2013 | Table 3.1 pins 60,158,177 ball number added. Pins 168,170 ball number modified. |
| 1.25 | 13/10/2013 | Section 4.1 CTS/RTS input/output definitions exchange. |
| 1.26 | 24/11/2013 | UART3_RTS strap-option hazard |
| 1.27 | 17/12/2013 | SOM features fix: Lineout is not exported. Headphones out is supported. |
| 1.28 | 16/02/2015 | Updated SOM Picture, Mechanical Drawing |

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1. Overview

1.1. General Information

The VAR-SOM-MX6 is a high performance System-on-Module. It provides an ideal building block that easily integrates with a wide range of target markets requiring rich multimedia functionality, powerful graphics and video capabilities, as well as high-processing power. Compact, cost effective and with low power consumption, VAR-SOM-MX6 secures an Intel Atom performance level.

Supporting products:

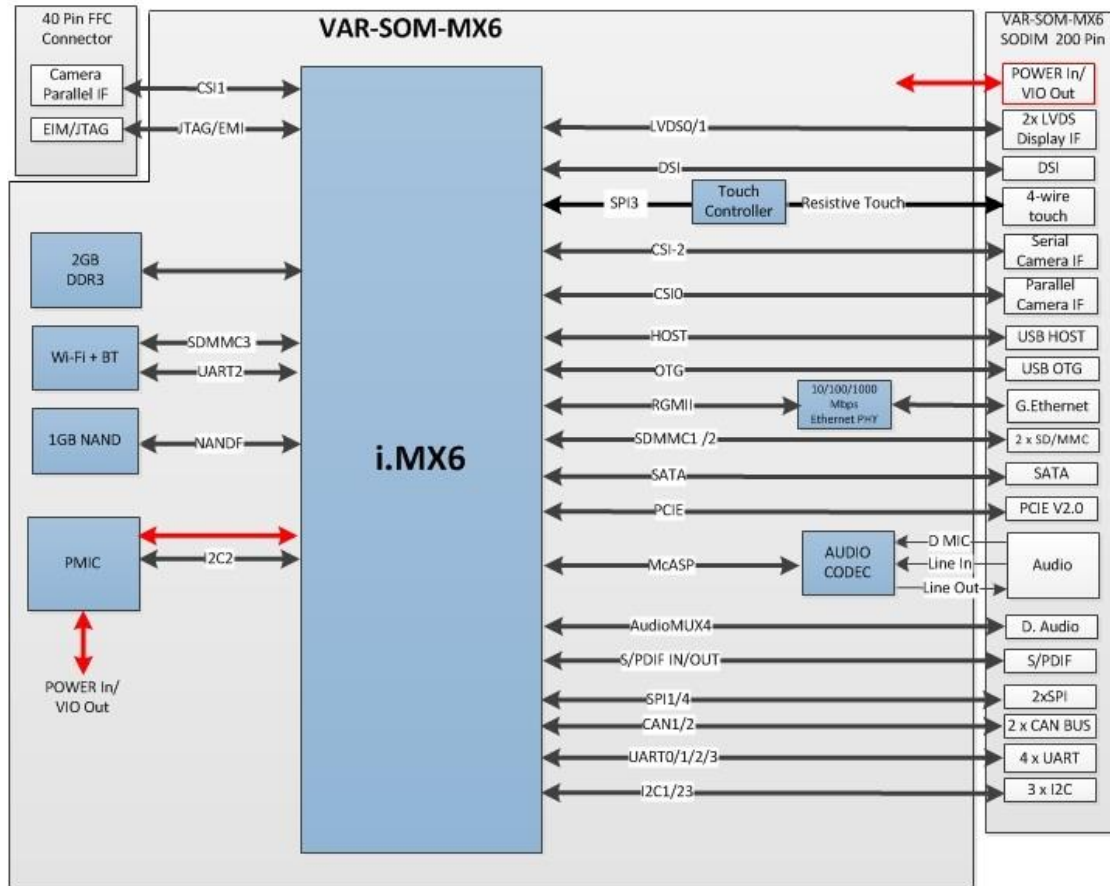
- VAR-MX6CustomBoard – evaluation board
 - ✓ Carrier -Board, compatible with VAR-SOM-MX6
 - ✓ Schematics
- VAR-EXT-CB402 – CSI2 Camera module
- O.S support
 - ✓ Linux BSP
 - ✓ Windows Embedded Compact 7
 - ✓ Android

Contact Variscite support services for further information: <mailto:support@variscite.com>.

1.2. Feature Summary

- Freescale i.MX6 series SoC (Single/Dual /Quad ARM® Cortex™-A9 Core, 1.2 GHz)
- Up to 16 Gb DDR3 RAM
- 8Gb NAND Flash for storage memory/boot
- 2 x LVDS display interface
- HDMI V1.4 interface
- 1 x MIPI DSI
- Touch panel interface
- Parallel & serial camera interface
- On-board 10/100/1000 Mbps Ethernet PHY
- WLAN (802.11 b/g/n) / BT
- 1 x USB 2.0 host, 1 x OTG
- 2 x SD/MMC
- Serial interfaces (SPI , I2C, UART, I2S,)
- CAN Bus
- Stereo line-In / headphones out
- Digital microphone
- Single 3.3 V power supply
- 67mm x 51mm, 200 pin SO-DIMM Connector

1.3. Block Diagram



2. Main Hardware Components

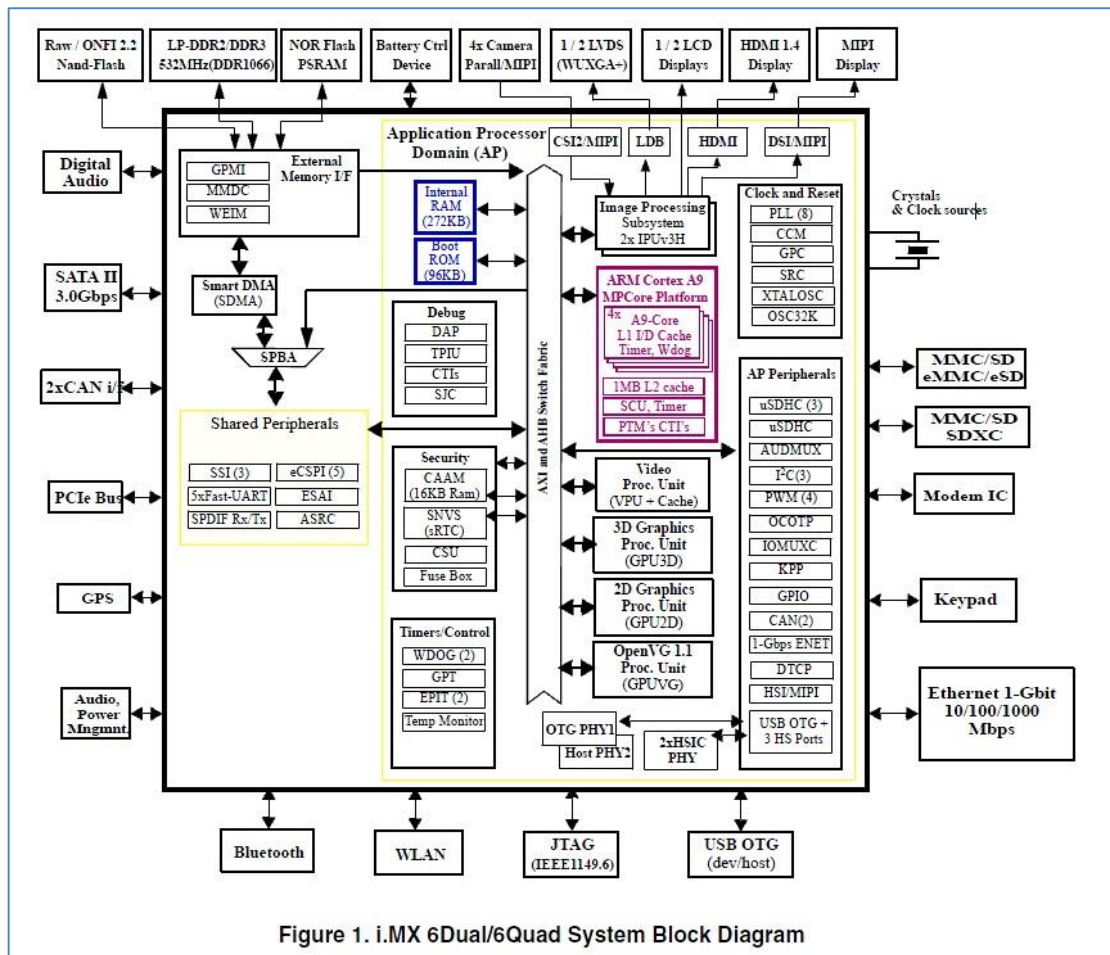
This section summarizes the main hardware building blocks of the VAR-SOM-MX6

2.1. Freescale i.MX6

2.1.1. Overview

The i.MX6Dual and i.MX6 Quad processors represent Freescale Semiconductor’s latest achievement in integrated multimedia applications processors, optimized for lowest power consumption. The processors feature Freescale’s advanced implementation of the quad ARM™ Cortex-A9 core, which operates at speeds of up to 1.2 GHz. They include 2D and 3D graphics processors, 3D 1080p video processing and integrated power management. Each processor provides a 64-bit DDR3/LVDDR3-1066 memory interface and a number of other interfaces such as WLAN, Bluetooth™, GPS, hard drive, displays, and camera sensors.

2.1.2. i.MX6 Block Diagram



2.1.3. CPU Platform

The i.MX6 Dual / Quad Application Processor (AP) is based on the ARM Cortex-A9 MPCore™ Platform, which has the following features:

- ARM Cortex A9 MPCore™ Dual or Quad core CPU configurations (with TrustZone)
- Symmetric CPU configuration where each CPU includes:
 - 32 Kbyte L1 Instruction Cache
 - 32 Kbyte L1 Data Cache
 - Private Timer and Watchdog
 - Cortex-A9 NEON MPE (Media Processing Engine) Co-processor.
- The ARM Cortex A9 MPCore™ complex includes:
 - General Interrupt Controller (GIC) with 128 interrupt support
 - Global Timer
 - Snoop Control Unit (SCU)
 - 1 Megabyte unified L2 cache shared by all CPU cores (Dual or Quad)
 - Two Master AXI (64-bit) bus interfaces output of L2 cache
- NEON MPE coprocessor
 - SIMD Media Processing Architecture
 - NEON register file with 32x64-bit general-purpose registers
 - NEON Integer execute pipeline (ALU, Shift, MAC)
 - NEON dual, single-precision floating point execute pipeline (FADD, FMUL)
 - NEON load/store and permute pipeline External
 - Supports single and double-precision add, subtract, multiply, divide, multiply and accumulate, and square root operations as described in the ARM VFPv3 architecture.
- Provides conversions between 16-bit, 32-bit and 64-bit floating-point formats and ARM integer word formats.

2.1.4. Memory Interfaces

The memory system consists of the following components:

- Level 1 Cache—32 KB Instruction, 32 KB Data cache per core
- Level 2 Cache—Unified instruction and data (1 MByte)
- On-Chip Memory:
 - Boot ROM, including HAB (96 KB)
 - Internal multimedia / shared, fast access RAM (OCRAM, 256 KB)
 - Secure/non-secure RAM (16 KB)
- External memory interfaces:
 - 16-bit, 32-bit, and 64-bit DDR3-1066, LV-DDR3-1066, and 1/2 LPDDR2-1066 channels, supporting DDR interleaving mode, for 2x32 LPDDR2-1066
 - 8-bit NAND-Flash, including support for Raw MLC/SLC, 2 KB, 4 KB, and 8 KB page size,
 - BA-NAND, PBA-NAND, LBA-NAND, OneNAND™ and others. BCH ECC up to 32 bit.
 - 16-bit NOR Flash. All WEIMv2 pins are muxed on other interfaces.
 - 16-bit PSRAM, Cellular RAM

2.1.5. DMA engine

The SDMA is multi-channel flexible DMA engine. It helps in maximizing system performance by off-loading the various cores in dynamic data routing. It has the following features:

- Powered by a 16-bit Instruction-Set micro-RISC engine
- Multi-channel DMA supporting up to 32 time-division multiplexed DMA channels
- 48 events with total flexibility to trigger any combination of channels
- Memory accesses including linear, FIFO, and 2D addressing
- Shared peripherals between ARM and SDMA
- Very fast Context-Switching with 2-level priority based preemptive multi-tasking
- DMA units with auto-flush and prefetch capability
- Flexible address management for DMA transfers (increment, decrement, and no address changes on source and destination address)
- DMA ports can handle unit-directional and bi-directional flows (copy mode)
- Up to 8-word buffer for configurable burst transfers
- Support of byte-swapping and CRC calculations
- Library of Scripts and API is available

2.1.6. Display Subsystem

The i.MX6Dual/6Quad video graphics subsystem consists of the following dedicated modules:

- Video Processing Unit (VPU): a multi-standard high performance video/image CODEC
- Three Graphics Processing Units (GPUs):
 - 3D GPU: accelerating the generation of 3D graphics (OpenGL/ES) and vector graphics (OpenVG)
 - 2D GPU: acceleration the generation of 2D graphics (BitBLT).
 - OpenVG: acceleration of vector graphics (OpenVG).
- Two (identical) Image Processing Units (IPUs): providing connectivity to cameras and displays, related processing, synchronization and control.
- Display interface bridges: providing optional translation from the digital display interface supported by the IPU to other interfaces:
 - LVDS bridge (LDB): providing up to two LVDS interfaces
 - HDMI transmitter
 - MIPI/DSI transmitter
- MIPI/CSI-2 receiver
- Two (identical) Display Content Integrity Checker (DCIC) are used to authenticate sensitive displayed data.
- A Video Data Order Adapter (VDOA): used to re-order video data from the "tiled" order used by the VPU to the conventional raster-scan order needed by the IPU.

2.1.7. MIPI - Camera Serial Interface Host Controller

The MIPI CSI-2 Host Controller supports the following features:

- Compliant with MIPI Alliance Standard for Camera Serial Interface 2 (CSI-2), Version 1.00 - 29 November 2005
- Optional support for Camera Control Interface (CCI) through the use of DesignWare Core (DW_apb_i2c)
- Interface with MIPI D-PHY following PHY Protocol Interface (PPI), as defined in MIPI Alliance Specification for D-PHY, Version 1.00.00 - 14 May 2009
- Supports up to 4 D-PHY Rx Data Lanes
- Dynamically configurable multi-lane merging
- Long and Short packet decoding
- Timing accurate signaling of Frame and Line synchronization packets; Support for several frame formats such as:
 - General Frame or Digital Interlaced Video with or without accurate sync timing
 - Data type (Packet or Frame level) and Virtual Channel interleaving
- 32-bit Image Data Interface delivering data formatted as recommended in CSI-2 Specification
- Supports all primary and secondary data formats:
 - RGB, YUV and RAW color space definitions
 - From 24-bit down to 6-bit per pixel
 - Generic or user-defined byte-based data types
 - Error detection and correction
 - PHY level
 - Packet level
 - Line level
 - Frame level

2.1.8. 2D and 3D Graphics Processing Unit (GPU)

The GPU2D module has two independent sub-modules: R2D and V2D GPUs. Both GPU were designed to display on a variety of consumer devices. Addressable screen sizes range from small displays featured on cell phones to large 1080p high definition displays.

The GPU2D cores provide powerful graphics at low power consumption, utilizing the smallest silicon footprints. Dynamic power consumption is minimized by extensive use of localized clock gating.

Hardware acceleration is brought to numerous 2D and VG applications including graphical user interfaces (GUI), menu displays, flash animation and gaming.

The GPU3D is a high-performance core that delivers hardware acceleration for 3D graphics display. Addressable screen sizes range from the smallest cell phones to HD 1080p displays. It provides high performance, high quality graphics, low power consumption and the smallest silicon footprint.

GPU3D accelerates numerous 3D graphics applications, including Graphical User Interfaces (GUI), menu displays, flash animation, and gaming. This module supports the following graphics APIs:

- OpenGL ES 2.0
- OpenGL ES 1.1
- OpenVG 1.1
- EGL 1.4
- DirectX 11_9_3

- OpenGL 2.1 and 3.0
- OpenCL 1.1 E

2.1.9. Audio Back End

The AUDMUX provides flexible, programmable routing of the serial interfaces (SSI1 or SSI2) to and from off-chip devices. The AUDMUX routes audio data (and even splices together multiple time-multiplexed audio streams) but does not decode or process audio data itself. The AUDMUX is controlled by the ARM but can route data even when the ARM is in a low-power mode.

The ESAI (Enhanced Serial Audio Interface) provides a full-duplex serial port for serial communication with a variety of serial devices, including industry-standard codecs, SPDIF transceivers, and other processors. The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator. The ESAI is connected to the IOMUX and to the ESAI_BIFIFO module.

The ESAI_BIFIFO (ESAI Bus Interface and FIFO) is the interface between the ESAI module and the shared peripheral bus. It contains the FIFOs used to buffer data to and from the ESAI, as well as providing the data word alignment and padding necessary to match the 24-bit data bus of the ESAI to the 32-bit data bus of the shared peripheral bus.

The SPDIF (Sony/Philips Digital Interface) audio module is a stereo transceiver that allows the processor to receive and transmit digital audio over it. The SPDIF receiver section includes a frequency measurement block that allows the precise measurement of incoming sampling frequency. A recovered clock is provided by the SPDIF receiver section and may be used to drive both internal and external components in the system. The SPDIF is connected to the shared peripheral bus.

The ASRC (Asynchronous Sample Rate Converter) converts the sampling rate of a signal associated to an input clock into a signal associated to a different output clock. The ASRC supports concurrent sample rate conversions of up to 10 channels of over 120dB THD+N. The sample rate conversion of each channel is associated to a pair of incoming and outgoing sampling rates. The ASRC supports up to three sampling rate pairs. The ASRC is connected to the shared peripheral bus.

2.1.10. 10/100/1000 Ethernet Controller

The MAC-NET core, in conjunction with a 10/100/1000 MAC, implements layer 3 network acceleration functions. These functions are designed to accelerate the processing of various common networking protocols, such as IP, TCP, UDP and ICMP, providing wire speed services to client applications. The MAC operation is fully programmable and can be used in NIC (Network Interface Card), bridging, or switching applications. The core implements the remote network monitoring (RMON) counters according to IETF RFC 2819. The core also implements a hardware acceleration block to optimize the performance of network controllers providing IP and TCP, UDP, ICMP protocol services. The acceleration block performs critical functions in hardware, which are typically implemented with large software overhead. The core implements programmable embedded FIFOs that can provide buffering on the receive path for loss-less flow control. Advanced power management features are available with magic packet detection and programmable power-down modes.

2.2. Memory

2.2.1. RAM

The VAR-SOM-MX6 is available with up to 16 Gb of DDR3 memory.

2.2.2. Non-volatile Storage Memory

The VAR-SOM-MX6 is available with up to 8Gb of SLC NAND FLASH memory. The NAND flash is used for Flash Disk purposes, O.S. run-time-image and the Boot-loader (Boot from NAND). First block (block address 00h) of the memory device is guaranteed to be valid without ECC (up to 1,000 PROGRAM/ERASE cycles)

2.3. 10/100/1000 Ethernet PHY

The VAR-SOM-MX6 features the Micrel KSZ9031 gigabit Ethernet PHY. The KSZ9031RN is a completely integrated triple speed (10Base-T/100Base-TX/1000Base-T) Ethernet Physical Layer Transceiver for transmission and reception of data over standard CAT-5 unshielded twisted pair (UTP) cable. The KSZ9031RN provides the Reduced Gigabit Media Independent Interface (RGMII) for direct connection to RGMII MACs in Gigabit Ethernet processors and switches for data transfer at 10/100/1000 Mbps speed.

2.4. TLV320AIC3106 Audio

The Texas Instrument's TLV320AIC3106 is a low-power, highly integrated stereo audio codec with stereo headphone amplifier, as well as multiple inputs and outputs programmable in single-ended or fully differential configurations. Extensive register-based power control is included, enabling stereo 48-kHz DAC playback as low as 15mW. The VAR-SOM-MX6 exposes the following interface of the TLV320AIC3106:

- Headphone
- Line-in
- Digital microphone

2.5. Wi-Fi + BT

Wi-Fi & Bluetooth connectivity is supported by an on-board module TiWi – BLE.

The TiWi-BLE module is a high performance 2.4 GHz IEEE 802.11 b/g/n Bluetooth 4.0 radio in a cost effective, pre-certified footprint.

The module realizes the necessary PHY/MAC layers to support WLAN applications in conjunction with a host processor over a SDIO interface.

The module also provides a Bluetooth platform through the HCI transport layer. Both WLAN and Bluetooth share the same antenna port.

2.6. PMIC

The VAR-SOM-MX6 features Freescale's PMPF0100 as a Power Management Integrated circuit (PMIC) designed specifically for use with Freescale's i.MX6 series of application processors. The PMPF0100 regulates all power rails required on SoM from a single 3.3 V power supply.

The PMIC is fully programmable via the I2C interface and associated register map. Additional communication is provided by direct logic interfacing including interrupt, watchdog and reset.

3. External Connectors

The VAR-SOM-MX6 exposes a 200-pin SO-DIMM mechanical standard interface. The recommended mating connector for baseboard interfacing is FCI 10033853-052FSLF or equivalent.

In addition to the 200-pin SO-DIMM interface VAR-SOM-MX6 exposes a 40-pin FFC connector. The recommended mating cable is Molex 21020-0427 or equivalent

Pin#:

Pin number on the SO-DIMM200 connector

Pin Name:

Default VAR-SOM-MX6 pin name

Type:

Pin type & direction:

- I – In
- O – Out
- DS – Differential Signal
- A – Analog
- Power – Power Pin

Pin Group:

Pin functionality group

i.MX6 Ball:

Ball number

Mode (Tables 3.2 & 3.4):

Pin mux mode option

3.1. VAR-SOM-MX6 Connector Pin-out

| Pin # | Pin Name | Type | Pin Group | GPIO | i.MX6 Ball |
|-------|--------------|-------|------------------------------|-----------|------------|
| 1 | GND | POWER | Digital GND | | |
| 2 | GND | POWER | Digital GND | | |
| 3 | MDI_A+ | DS | Gigabit Ethernet | | |
| 4 | MDI_C+ | DS | Gigabit Ethernet | | |
| 5 | MDI_A- | DS | Gigabit Ethernet | | |
| 6 | MDI_C- | DS | Gigabit Ethernet | | |
| 7 | GND | POWER | Digital GND | | |
| 8 | GND | POWER | Digital GND | | |
| 9 | MDI_B+ | DS | Gigabit Ethernet | | |
| 10 | MDI_D+ | DS | Gigabit Ethernet | | |
| 11 | MDI_B- | DS | Gigabit Ethernet | | |
| 12 | MDI_D- | DS | Gigabit Ethernet | | |
| 13 | GND | POWER | Digital GND | | |
| 14 | GND | POWER | Digital GND | | |
| 15 | GETH_LED2 | O | Gigabit Ethernet LED | | |
| 16 | GETH_LED1 | O | Gigabit Ethernet LED | | |
| 17 | PWM0 | IO | Pulse width modulation | GPIO4[30] | T25 |
| 18 | DMIC_CLK | O | Digital microphone interface | | |
| 19 | GND | POWER | Digital GND | | |
| 20 | DMIC_DATA | I | Digital microphone interface | | |
| 21 | AUDMUX4_RXD | IO | Digital audio mux | GPIO5[17] | W24 |
| 22 | AUDMUX4_RXC | IO | Digital audio mux | GPIO5[13] | U23 |
| 23 | AUDMUX4_RXFS | IO | Digital audio mux | GPIO5[12] | V25 |
| 24 | AUDMUX4_TXFS | IO | Digital audio mux | GPIO5[16] | V24 |
| 25 | AUDMUX4_TXC | IO | Digital audio mux | GPIO5[14] | U22 |
| 26 | AUDMUX4_TXD | IO | Digital audio mux | GPIO5[15] | T20 |
| 27 | GND | POWER | Digital GND | | |
| 28 | GND | POWER | Digital GND | | |
| 29 | CLKO2 | O | Reference clock out | | |
| 30 | NC | | Leave not connected | | |
| 31 | GND | POWER | Digital GND | | |
| 32 | VIN_3V3 | POWER | 3.3 V power supply IN | | |
| 33 | GND | POWER | Digital GND | | |
| 34 | VIN_3V3 | POWER | 3.3 V power supply IN | | |
| 35 | GND | POWER | Digital GND | | |
| 36 | VIN_3V3 | POWER | 3.3 V power supply IN | | |
| 37 | GND | POWER | Digital GND | | |
| 38 | VIN_3V3 | POWER | 3.3 V power supply IN | | |

VAR-SOM-MX6 SYSTEM ON MODULE

| Pin # | Pin Name | Type | Pin Group | GPIO | i.MX6 Ball |
|-------|------------|-------|---------------------------|-----------|------------|
| 39 | CSPI1_CS0 | IO | Configurable SPI | GPIO4[9] | U6 |
| 40 | BOOT_SEL1 | IO | EIM_DA13 | GPIO3[13] | M23 |
| 41 | CSPI1_MISO | IO | Configurable SPI | GPIO4[8] | U7 |
| 42 | BOOT_SEL0 | IO | EIM_DA7 | GPIO3[7] | L25 |
| 43 | CSPI1_CLK | IO | Configurable SPI | GPIO4[6] | W5 |
| 44 | CAN1_TX | IO | Controller area network | GPIO1[7] | R3 |
| 45 | CSPI1_MOSI | IO | Configurable SPI | GPIO4[7] | V6 |
| 46 | CAN1_RX | IO | Controller area network | GPIO1[8] | R5 |
| 47 | GND | POWER | Digital GND | | |
| 48 | CSPI1_CS1 | IO | Configurable SPI | GPIO4[10] | W6 |
| 49 | 3V3_PER | POWER | Power good indication | | |
| 50 | UART2_CTS | IO | UART2 port ^[2] | GPIO3[28] | G23 |
| 51 | UART2_RTS | IO | UART2 port ^[2] | GPIO3[29] | J19 |
| 52 | UART2_TXD | IO | UART2 port ^[2] | GPIO3[26] | E24 |
| 53 | UART2_RXD | IO | UART2 port ^[2] | GPIO3[27] | E25 |
| 54 | UART3_RXD | IO | UART3 port | GPIO3[25] | G22 |
| 55 | UART3_CTS | IO | UART3 port | GPIO3[23] | D25 |
| 56 | UART3_TXD | IO | UART3 port | GPIO3[24] | F22 |
| 57 | UART3_RTS | IO | UART3 port ^[3] | GPIO2[31] | F23 |
| 58 | GND | POWER | Digital GND | | |
| 59 | GND | POWER | Digital GND | | |
| 60 | SD2_CLK | IO | SD/MMC and SDXC | GPOP1[10] | C21 |
| 61 | SD2_DATA2 | IO | SD/MMC and SDXC | GPIO1[13] | A23 |
| 62 | SD2_DATA0 | IO | SD/MMC and SDXC | GPIO1[15] | A22 |
| 63 | SD2_DATA1 | IO | SD/MMC and SDXC | GPIO1[14] | E20 |
| 64 | SD2_CMD | O | SD/MMC and SDXC | GPIO1[11] | F19 |
| 65 | SD2_DATA3 | IO | SD/MMC and SDXC | GPIO1[12] | B22 |
| 66 | GND | POWER | Digital GND | | |
| 67 | GND | POWER | Digital GND | | |
| 68 | SD1_DATA0 | IO | SD/MMC and SDXC | GPIO1[16] | A21 |
| 69 | SD1_CMD | IO | SD/MMC and SDXC | GPIO1[18] | B21 |
| 70 | SD1_DATA2 | IO | SD/MMC and SDXC | GPIO1[19] | E19 |
| 71 | SD1_DATA1 | IO | SD/MMC and SDXC | GPIO1[17] | C20 |
| 72 | SD1_CLK | O | SD/MMC and SDXC | | |
| 73 | SD1_DATA3 | IO | SD/MMC and SDXC | GPIO1[21] | F18 |
| 74 | NC | | Leave not connected | | |
| 75 | SPDIFIN | IO | SPDIF | GPIO3[21] | H20 |
| 76 | GND | POWER | Digital GND | | |
| 77 | SPDIFOUT | IO | SPDIF | GPIO3[22] | E23 |

VAR-SOM-MX6 SYSTEM ON MODULE

| Pin # | Pin Name | Type | Pin Group | GPIO | i.MX6 Ball |
|-------|----------------|-------|-----------------------|-----------|------------|
| 78 | GND | POWER | Digital GND | | |
| 79 | USB_H1_OC | IO | USB host | GPIO3[30] | J20 |
| 80 | CAN2_TX_OTG_OC | IO | FlexCAN-2 | GPIO4[14] | T6 |
| 81 | CSI0_HSYNCH | IO | Camera interface | GPIO5[19] | P4 |
| 82 | CAN2_RX | IO | FlexCAN-2 | GPIO4[15] | V5 |
| 83 | UART1_RX | IO | UART1 port | GPIO5[29] | M3 |
| 84 | UART1_RTS | IO | UART1 port | GPIO3[20] | G20 |
| 85 | UART1_TX | IO | UART1 port | GPIO5[28] | M1 |
| 86 | UART1_CTS | IO | UART1 port | GPIO3[19] | G21 |
| 87 | I2C1_SDA | IO | I2C interface | GPIO5[26] | N6 |
| 88 | I2C1_SCL | IO | I2C interface | GPIO5[27] | N5 |
| 89 | GND | POWER | Digital GND | | |
| 90 | I2C3_SDA | IO | I2C interface | GPIO7[11] | R2 |
| 91 | SATA_RXN | DS | Serial ATA | | A14 |
| 92 | I2C3_SCL | IO | I2C interface | GPIO1[5] | R4 |
| 93 | SATA_RXP | DS | Serial ATA | | B14 |
| 94 | USB_OTG_ID | IO | USB on-the-go | GPIO1[4] | R6 |
| 95 | GND | POWER | Digital GND | | |
| 96 | CSI0_DAT19 | IO | Camera interface | GPIO6[5] | L6 |
| 97 | SATA_TXP | DS | Serial ATA | | A12 |
| 98 | POR_B | I | Reset | | C11 |
| 99 | SATA_TXN | DS | Serial ATA | | B12 |
| 100 | CLK1_N | DS | PCIE clock | | C7 |
| 101 | GND | POWER | Digital GND | | |
| 102 | CLK1_P | DS | PCIE clock | | D7 |
| 103 | VIN_3V3 | POWER | Main power supply | | G15 |
| 104 | USB_H1_VBUS | I | USB 2.0 5V indication | | D10 |
| 105 | VIN_3V3 | POWER | Main power supply | | G15 |
| 106 | USB_OTG_VBUS | I | OTG 5V indication | | E9 |
| 107 | VIN_3V3 | POWER | Main power supply | | G15 |
| 108 | USB_HOST_DN | DS | USB host | | F10 |
| 109 | VIN_3V3 | POWER | Main power supply | | G15 |
| 110 | USB_HOST_DP | DS | USB host | | E10 |
| 111 | VIN_3V3 | POWER | Main power supply | | G15 |
| 112 | GND | POWER | Digital GND | | |
| 113 | CSI0_DAT18 | IO | Camera interface | GPIO6[4] | M6 |
| 114 | USB_OTG_DN | DS | USB on-the-go | | B6 |
| 115 | CSI0_DAT15 | IO | Camera interface | GPIO6[1] | M5 |
| 116 | USB_OTG_DP | DS | USB on-the-go | | A6 |
| 117 | CSI0_DAT17 | IO | Camera interface | GPIO6[3] | L3 |

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| Pin # | Pin Name | Type | Pin Group | GPIO | i.MX6 Ball |
|-------|--------------|-------|--------------------------|-----------|------------|
| 118 | GND | POWER | Digital GND | | |
| 119 | CSI_D0P | DS | Camera serial interface | | E3 |
| 120 | CSI0_VSYNC | IO | Camera interface | GPIO5[21] | N2 |
| 121 | CSI_D0M | DS | Camera serial interface | | E4 |
| 122 | CSI0_DATA_EN | IO | Camera interface | GPIO5[20] | P3 |
| 123 | CSI_D1M | DS | Camera serial interface | | D1 |
| 124 | CSI0_DAT12 | IO | Camera interface | GPIO5[30] | M2 |
| 125 | CSI_D1P | DS | Camera serial interface | | D2 |
| 126 | GND | POWER | Digital GND | | |
| 127 | CSI_D2P | DS | Camera serial interface | | E2 |
| 128 | PCIE_TXM | DS | PCI express interface | | A3 |
| 129 | CSI_D2M | DS | Camera serial interface | | E1 |
| 130 | PCIE_TXP | DS | PCI express interface | | B3 |
| 131 | CSI_D3M | DS | Camera serial interface | | F2 |
| 132 | GND | POWER | Digital GND | | |
| 133 | CSI_D3P | DS | Camera serial interface | | F1 |
| 134 | PCIE_RXP | DS | PCI express interface | | B2 |
| 135 | CSI_CLK0P | DS | Camera serial interface | | F3 |
| 136 | PCIE_RXM | DS | PCI express interface | | B1 |
| 137 | CSI_CLK0M | DS | Camera serial interface | | F4 |
| 138 | GND | POWER | Digital GND | | |
| 139 | GND | POWER | Digital GND | | |
| 140 | DSI_CLK0P | DS | Display serial interface | | H4 |
| 141 | DSI_D0M | DS | Display serial Interface | | G2 |
| 142 | DSI_CLK0M | DS | Display serial interface | | H3 |
| 143 | DSI_D0P | DS | Display serial interface | | G1 |
| 144 | GND | POWER | Digital GND | | |
| 145 | DSI_D1M | DS | Display serial interface | | H2 |
| 146 | HDMI_D1P | DS | HDMI | | J4 |
| 147 | DSI_D1P | DS | Display serial interface | | H1 |
| 148 | HDMI_D1M | DS | HDMI | | J3 |
| 149 | GND | POWER | Digital GND | | |
| 150 | HDMI_CLKM | DS | HDMI | | J5 |
| 151 | HDMI_D2P | DS | HDMI | | K4 |
| 152 | HDMI_CLKP | DS | HDMI | | J6 |
| 153 | HDMI_D2M | DS | HDMI | | K3 |
| 154 | HDMI_HPD | DS | HDMI | | K1 |
| 155 | HDMI_D0P | DS | HDMI | | K6 |
| 156 | HDMI_DDCCEC | IO | HDMI | | K2 |
| 157 | HDMI_D0M | DS | HDMI | | K5 |

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| Pin # | Pin Name | Type | Pin Group | GPIO | i.MX6 Ball |
|-------|-------------|-------|------------------------------|-----------|------------|
| 158 | GND | POWER | Digital GND | | |
| 159 | GND | POWER | Digital GND | | |
| 160 | LVDS0_TX1_N | DS | LVDS display bridge | | U4 |
| 161 | LVDS0_TX0_N | DS | LVDS display bridge | | U2 |
| 162 | LVDS0_TX1_P | DS | LVDS display bridge | | U3 |
| 163 | LVDS0_TX0_P | DS | LVDS display bridge | | U1 |
| 164 | LVDS0_TX2_N | DS | LVDS display bridge | | V2 |
| 165 | LVDS0_TX3_N | DS | LVDS display bridge | | W2 |
| 166 | LVDS0_TX2_P | DS | LVDS display bridge | | V1 |
| 167 | LVDS0_TX3_P | DS | LVDS display bridge | | W1 |
| 168 | LVDS0_CLK_N | DS | LVDS display bridge | | V4 |
| 169 | GND | POWER | Digital GND | | |
| 170 | LVDS0_CLK_P | DS | LVDS display bridge | | V3 |
| 171 | CSI0_DAT14 | IO | Camera interface | GPIO6[0] | M4 |
| 172 | GND | POWER | Digital GND | | |
| 173 | CSI0_DAT16 | IO | Camera interface | GPIO6[2] | L4 |
| 174 | I2C2_SCL | IO | I2C interface ^[1] | | U5 |
| 175 | CSI0_DAT13 | IO | Camera interface | GPIO5[31] | L1 |
| 176 | I2C2_SDA | IO | I2C interface ^[1] | | T7 |
| 177 | CSI0_PIXCLK | I | Camera interface | GPIO5[18] | P1 |
| 178 | GND | POWER | Digital GND | | |
| 179 | GND | POWER | Digital GND | | |
| 180 | LVDS1_CLK_N | DS | LVDS display bridge | | Y3 |
| 181 | LVDS1_TX3_P | DS | LVDS display bridge | | AA4 |
| 182 | LVDS1_CLK_P | DS | LVDS display bridge | | Y4 |
| 183 | LVDS1_TX3_N | DS | LVDS display bridge | | AA3 |
| 184 | LVDS1_TX0_N | DS | LVDS display bridge | | Y1 |
| 185 | GND | POWER | Digital GND | | |
| 186 | LVDS1_TX0_P | DS | LVDS display bridge | | Y2 |
| 187 | TS_X- | AI | Touch screen interface | | |
| 188 | LVDS1_TX1_N | DS | LVDS display bridge | | AA1 |
| 189 | TS_X+ | AI | Touch screen interface | | |
| 190 | LVDS1_TX1_P | DS | LVDS display bridge | | AA2 |
| 191 | TS_Y+ | AI | Touch screen interface | | |
| 192 | LVDS1_TX2_N | DS | LVDS display bridge | | AB1 |
| 193 | TS_Y- | AI | Touch screen interface | | |
| 194 | LVDS1_TX2_P | DS | LVDS display bridge | | AB2 |
| 195 | AGND | POWER | Audio GND | | |
| 196 | AGND | POWER | Audio GND | | |
| 197 | LINEIN1_LP | AI | | | |

| Pin # | Pin Name | Type | Pin Group | GPIO | i.MX6 Ball |
|-------|------------|------|-----------|------|------------|
| 198 | HPLOUT | AO | | | |
| 199 | LINEIN1_RP | AI | | | |
| 200 | HPROUT | AO | | | |

Notes:

- [1] I2C2 Interface is used on-som. Pin mode can't be changed.
- [2] UART2 interface is used for on-board Bluetooth connectivity. Pin can't be used and mode can't be altered if the Bluetooth is enabled.
- [3] UART3 RTS pin is being latched at boot to determine boot sequence. Use with OE# buffer, and enable only after SOM is powered-up. Use reference schematics as example.

3.2. SO-DIMM 200 Pin Mux

The table below summarizes the additional available functionality for each pin-in SO-DIMM 200 connector.

| PIN | MODE 0 | MODE 1 | MODE 2 | MODE 3 | MODE 4 | MODE 5 | MODE 6 | MODE 7 |
|-----|-------------------------|-------------------------------|----------------------|-------------------------------------|-------------------------------------|---------------|---------------------|--|
| 16 | | ENET. TX_EN | ESAI. TX3_RX2 | | | GPIO1 [28] | SATA_PHY. TDI | ANATOP. USBPHY2_TSTO_R X_SQUELCH |
| 17 | IPU1. DISPO_DATA[9] | IPU2. DISPO_DATA[9] | PWM2. PWMO | WDOG2. WDOG_B | SDMA. DEBUG_EVENT_C HANNEL[2] | GPIO4 [30] | MMDC_DEBUG[14] | PL301_MX63PER1 . HADDR[20] |
| 21 | IPU1. DISPO_DATA[23] | IPU2. DISPO_DATA[23] | ECSPI1. SSO | AUDMUX. AUD4_RXD | SDMA. DEBUG_BUS_DEV ICE[2] | GPIO5 [17] | MMDC_DEBUG[28] | PL301_MX63PER1 . HADDR[31] |
| 22 | IPU1. DISPO_DATA[19] | IPU2. DISPO_DATA[19] | ECSPI2. SCLK | AUDMUX. AUD5_RXD | AUDMUX. AUD4_RXC | GPIO5 [13] | MMDC_DEBUG[24] | WEIM_CS[3] |
| 23 | IPU1. DISPO_DATA[18] | IPU2. DISPO_DATA[18] | ECSPI2. SSO | AUDMUX. AUD5_TXFS | AUDMUX. AUD4_RXFS | GPIO5 [12] | MMDC_DEBUG[23] | WEIM_CS[2] |
| 24 | IPU1. DISPO_DATA[22] | IPU2. DISPO_DATA[22] | ECSPI1. MISO | AUDMUX. AUD4_TXFS | SDMA. DEBUG_BUS_DEV ICE[1] | GPIO5 [16] | MMDC_DEBUG[27] | PL301_MX63PER1 . HADDR[30] |
| 25 | IPU1. DISPO_DATA[20] | IPU2. DISPO_DATA[20] | ECSPI1. SCLK | AUDMUX. AUD4_TXC | SDMA. DEBUG_EVT_CHN _LINES[7] | GPIO5 [14] | MMDC_DEBUG[25] | PL301_MX63PER1 . HADDR[28] |
| 26 | IPU1. DISPO_DATA[21] | IPU2. DISPO_DATA[21] | ECSPI1. MOSI | AUDMUX. AUD4_TXD | SDMA. DEBUG_BUS_DEV ICE[0] | GPIO5 [15] | MMDC_DEBUG[26] | PL301_MX63PER1 . HADDR[29] |
| 39 | ECSPI1. SSO | ENET. COL | AUDMUX. AUD5_RXD | KPP. ROW[1] | UART5. RXD_MUX | GPIO4 [9] | USDHC2. VSELECT | PL301_MX63PER1 . HADDR[2] |
| 40 | WEIM_DATA[13] | IPU1. DI1_DO_CS | CCM. DI1_EXT_CLK | MIPI_CORE. DPHY_TEST_ OUT[15] | SDMA. DEBUG_EVT_CHN _LINES[4] | GPIO3 [13] | TPSMP. HDATA[27] | SRC. BT_CFG[13] |
| 41 | ECSPI1. MISO | ENET. MDIO | AUDMUX. AUD5_TXFS | KPP. COL[1] | UART5. TXD_MUX | GPIO4 [8] | USDHC1. VSELECT | PL301_MX63PER1 . HADDR[1] |
| 43 | ECSPI1. SCLK | ENET. RDATA[3] | AUDMUX. AUD5_TXC | KPP. COL[0] | UART4. TXD_MUX | GPIO4 [6] | DCIC1. DCIC_OUT | SRC. ANY_PU_RST |
| 44 | ESAI. TX4_RX1 | ECSPI5. RDY | EPIT1. EPITO | CAN1. TXCAN | UART2. TXD_MUX | GPIO1 [7] | SPDIF. PLOCK | USBOH3. OTGUSB_HOST_M ODE |
| 45 | ECSPI1. MOSI | ENET. TDATA[3] | AUDMUX. AUD5_TXD | KPP. ROW[0] | UART4. RXD_MUX | GPIO4 [7] | DCIC2. DCIC_OUT | PL301_MX63PER1 . HADDR[0] |
| 46 | ESAI. TX5_RX0 | ANATOP. ANATOP_32K_ OUT | EPIT2. EPITO | CAN1. RXCAN | UART2. RXD_MUX | GPIO1 [8] | SPDIF. SRCLK | USBOH3. OTGUSB_PWRCTL _WAKEUP |

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| PIN | MODE 0 | MODE 1 | MODE 2 | MODE 3 | MODE 4 | MODE 5 | MODE 6 | MODE 7 |
|-----|-----------------|--------------------|------------------------------------|------------------|------------------------------------|-----------|----------------------------|-------------------------|
| 48 | ECSPI1.SS1 | ENET.RDATA[2] | CAN1.TXCAN | KPP.COL[2] | ENET.MDC | GPIO4[10] | USBOH3.H1USB_PWRCTL_WAKEUP | PL301_MX63PER1.HADDR[3] |
| 50 | WEIM_D[28] | I2C1.SDA | ECSPI4.MOSI | IPU2.CSI1_D[12] | UART2.CTS | GPIO3[28] | IPU1.EXT_TRIG | IPU1.DIO_PIN13 |
| 51 | WEIM_D[29] | IPU1.DI1_PIN15 | ECSPI4.SS0 | | UART2.RTS | GPIO3[29] | IPU2.CSI1_VSYNC | IPU1.DIO_PIN14 |
| 52 | WEIM_D[26] | IPU1.DI1_PIN11 | IPU1.CSI0_D[1] | IPU2.CSI1_D[14] | UART2.TXD_MUX | GPIO3[26] | IPU1.SISG[2] | |
| 53 | WEIM_D[27] | IPU1.DI1_PIN13 | IPU1.CSI0_D[0] | IPU2.CSI1_D[13] | UART2.RXD_MUX | GPIO3[27] | IPU1.SISG[3] | |
| 54 | WEIM_D[25] | ECSPI4.SS3 | UART3.RXD_MUX | ECSPI1.SS3 | ECSPI2.SS3 | GPIO3[25] | AUDMUX.AUD5_RXC | UART1.DSR |
| 55 | WEIM_D[23] | IPU1.DIO_D0_CS | UART3.CTS | UART1.DCD | IPU2.CSI1_DATA_EN | GPIO3[23] | IPU1.DI1_PIN2 | IPU1.DI1_PIN14 |
| 56 | WEIM_EB[24] | ECSPI4.SS2 | UART3.TXD_MUX | ECSPI1.SS2 | ECSPI2.SS2 | GPIO3[24] | AUDMUX.AUD5_RXFS | UART1.DTR |
| 57 | WEIM_EB[3] | ECSPI4.RDY | UART3.RTS | UART1.RI | IPU2.CSI1_HSYNC | GPIO2[31] | IPU1.DI1_PIN3 | SRC.BT_CFG[31] |
| 61 | USDHC2.DAT2 | ECSPI5.SS1 | WEIM_CS[3] | AUDMUX.AUD4_TXD | KPP.ROW[6] | GPIO1[13] | CCM.STOP | ANATOP_TESTO[1] |
| 62 | USDHC2.DAT0 | ECSPI5.MISO | | AUDMUX.AUD4_RXD | KPP.ROW[7] | GPIO1[15] | DCIC2.DCIC_OUT | ANATOP_TESTO[2] |
| 63 | USDHC2.DAT1 | ECSPI5.SS0 | WEIM_CS[2] | AUDMUX.AUD4_TXFS | KPP.COL[7] | GPIO1[14] | CCM.WAIT | ANATOP_TESTO[0] |
| 64 | USDHC2.CMD | ECSPI5.MOSI | KPP.ROW[5] | AUDMUX.AUD4_RXC | PCIE_CTRL.DIAG_STATUS_B_US_MUX[10] | GPIO1[11] | | |
| 65 | USDHC2.DAT3 | ECSPI5.SS3 | KPP.COL[6] | AUDMUX.AUD4_TXC | PCIE_CTRL.DIAG_STATUS_B_US_MUX[11] | GPIO1[12] | SJC.DONE | ANATOP_TESTO[3] |
| 68 | USDHC1.DAT0 | ECSPI5.MISO | CAAM_WRA_PPER.RNG_OSC_OBS | GPT.CAPIN1 | PCIE_CTRL.DIAG_STATUS_B_US_MUX[8] | GPIO1[16] | HDMI_TX.OPHYDTB[1] | ANATOP_TESTO[7] |
| 69 | USDHC1.CMD | ECSPI5.MOSI | PWM4.PWMO | GPT.CMPOUT1 | | GPIO1[18] | | ANATOP_TESTO[5] |
| 70 | USDHC1.DAT2 | ECSPI5.SS1 | GPT.CMPOUT2 | PWM2.PWMO | WDOG1.WDOG_B | GPIO1[19] | WDOG1.WDOG_RST_B_DEB | ANATOP_TESTO[4] |
| 71 | USDHC1.DAT1 | ECSPI5.SS0 | PWM3.PWMO | GPT.CAPIN2 | PCIE_CTRL.DIAG_STATUS_B_US_MUX[7] | GPIO1[17] | HDMI_TX.OPHYDTB[0] | ANATOP_TESTO[8] |
| 73 | USDHC1.DAT3 | ECSPI5.SS2 | GPT.CMPOUT3 | PWM1.PWMO | WDOG2.WDOG_B | GPIO1[21] | WDOG2.WDOG_RST_B_DEB | ANATOP_TESTO[6] |
| 75 | WEIM_D[21] | ECSPI4.SCLK | IPU1.DIO_PIN17 | IPU2.CSI1_D[11] | USBOH3.USBOTG_OC | GPIO3[21] | I2C1.SCL | SPDIF.IN1 |
| 77 | WEIM_D[22] | ECSPI4.MISO | IPU1.DIO_PIN1 | IPU2.CSI1_D[10] | USBOH3.USBOTG_PWR | GPIO3[22] | SPDIF.OUT1 | PL301_MX63PER1.HWRITE |
| 79 | WEIM_D[30] | IPU1.DISP1_DAT[21] | IPU1.DIO_PIN11 | IPU1.CSI0_D[3] | UART3.CTS | GPIO3[30] | USBOH3.USBH1_OC | PL301_MX63PER1.HPROT[0] |
| 80 | CAN2.TXCAN | IPU1.SISG[4] | USBOH3.USBOTG_OC | KPP.COL[4] | UART5.RTS | GPIO4[14] | MMDC_DEBUG[49] | PL301_MX63PER1.HADDR[7] |
| 81 | IPU1.CSI0_HSYNC | | PCIE_CTRL.DIAG_STATUS_B_US_MUX[13] | CCM.CLKO | SDMA.DEBUG_PC[1] | GPIO5[19] | MMDC_DEBUG[30] | CHEETAH.TRCTL |
| 82 | CAN2.RXCAN | IPU1.SISG[5] | USBOH3.USBOTG_PWR | KPP.ROW[4] | UART5.CTS | GPIO4[15] | MMDC_DEBUG[50] | PL301_MX63PER1.HADDR[8] |
| 83 | IPU1.CSI0_D[11] | AUDMUX.AUD3_RXFS | ECSPI2.SS0 | UART1.RXD_MUX | SDMA.DEBUG_PC[5] | GPIO5[29] | MMDC_DEBUG[34] | CHEETAH.TRACE[8] |
| 84 | WEIM_D[20] | ECSPI4.SS0 | IPU1.DIO_PIN16 | IPU2.CSI1_D[15] | UART1.RTS | GPIO3[20] | EPIT2.EPITO | |
| 85 | IPU1.CSI0_D[10] | AUDMUX.AUD3_RXC | ECSPI2.MISO | UART1.TXD_MUX | SDMA.DEBUG_PC[4] | GPIO5[28] | MMDC_DEBUG[33] | CHEETAH.TRACE[7] |
| 86 | WEIM_D[19] | ECSPI1.SS1 | IPU1.DIO_PIN8 | IPU2.CSI1_D[16] | UART1.CTS | GPIO3[19] | EPIT1.EPITO | PL301_MX63PER1.HRESP |
| 87 | IPU1.CSI0_D[8] | WEIM_D[6] | ECSPI2.SCLK | KPP.COL[7] | I2C1.SDA | GPIO5[26] | MMDC_DEBUG[47] | CHEETAH.TRACE[5] |

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| PIN | MODE 0 | MODE 1 | MODE 2 | MODE 3 | MODE 4 | MODE 5 | MODE 6 | MODE 7 |
|-----|----------------------------|--|---|-------------------|------------------------------|---------------|--------------------|---------------------------------------|
| 88 | IPU1. CSIO_D[9] | WEIM_D[7] | ECSPi2. MOSI | KPP. ROW[7] | I2C1. SCL | GPIO5 [27] | MMDC_DEBUG[48] | CHEETAH. TRACE[6] |
| 90 | ESAI. TX3_RX2 | ENET. 1588_EVENT 2_IN | ENET. ANATOP_ET HERNET_REF _OUT | USDHC1. LCTL | SPDIF. IN1 | GPIO7 [11] | I2C3. SDA | SJC. DE_B |
| 92 | ESAI. TX2_RX3 | OBSERVE_M UX. OBSRV_INT_ OUT4 | KPP. ROW[7] | CCM. CLKO | CSU. CSU_ALARM_AUT [2] | GPIO1 [5] | I2C3. SCL | CHEETAH. EVENTI |
| 94 | ANATOP. USBOTG_I D | ENET. RX_ER | ESAI. HCKR | SPDIF. IN1 | ENET. 1588_EVENT2_O UT | GPIO1 [24] | PHY. TDI | ANATOP. USBPHY1_TSTO_R X_HS_RXD |
| 96 | IPU1. CSIO_D[19] | WEIM_D[15] | PCIE_CTRL. DIAG_STATU S_BUS_MUX [23] | UART5. CTS | SDMA. DEBUG_PC[13] | GPIO6 [5] | MMDC_DEBUG[42] | ANATOP_TESTO[9] |
| 113 | IPU1. CSIO_D[18] | WEIM_D[14] | PCIE_CTRL. DIAG_STATU S_BUS_MUX [22] | UART5. RTS | SDMA. DEBUG_PC[12] | GPIO6 [4] | MMDC_DEBUG[41] | CHEETAH. TRACE[15] |
| 115 | IPU1. CSIO_D[15] | WEIM_D[11] | PCIE_CTRL. DIAG_STATU S_BUS_MUX [19] | UART5. RXD_MUX | SDMA. DEBUG_PC[9] | GPIO6 [1] | MMDC_DEBUG[38] | CHEETAH. TRACE[12] |
| 117 | IPU1. CSIO_D[17] | WEIM_D[13] | PCIE_CTRL. DIAG_STATU S_BUS_MUX [21] | UART4. CTS | SDMA. DEBUG_PC[11] | GPIO6 [3] | MMDC_DEBUG[40] | CHEETAH. TRACE[14] |
| 120 | IPU1. CSIO_VSYN C | WEIM_D[1] | PCIE_CTRL. DIAG_STATU S_BUS_MUX [15] | | SDMA. DEBUG_PC[3] | GPIO5 [21] | MMDC_DEBUG[32] | CHEETAH. TRACE[0] |
| 122 | IPU1. CSIO_DATA _EN | WEIM_D[0] | PCIE_CTRL. DIAG_STATU S_BUS_MUX [14] | | SDMA. DEBUG_PC[2] | GPIO5 [20] | MMDC_DEBUG[31] | CHEETAH. TRCLK |
| 124 | IPU1. CSIO_D[12] | WEIM_D[8] | PCIE_CTRL. DIAG_STATU S_BUS_MUX [16] | UART4. TXD_MUX | SDMA. DEBUG_PC[6] | GPIO5 [30] | MMDC_DEBUG[35] | CHEETAH. TRACE[9] |
| 171 | IPU1. CSIO_D[14] | WEIM_D[10] | PCIE_CTRL. DIAG_STATU S_BUS_MUX [18] | UART5. TXD_MUX | SDMA. DEBUG_PC[8] | GPIO6 [0] | MMDC_DEBUG[37] | CHEETAH. TRACE[11] |
| 173 | IPU1. CSIO_D[16] | WEIM_D[12] | PCIE_CTRL. DIAG_STATU S_BUS_MUX [20] | UART4. RTS | SDMA. DEBUG_PC[10] | GPIO6 [2] | MMDC_DEBUG[39] | CHEETAH. TRACE[13] |
| 174 | ECSPi1_SS 3 | ENET_CRS | HDMI_TX_D DC_SCL | KEY_COL3 | I2C2_SCL | GPIO4 [12] | SPDIF_IN | CHEETAH. TRACE[10] |
| 175 | IPU1. CSIO_D[13] | WEIM_D[9] | PCIE_CTRL. DIAG_STATU S_BUS_MUX [17] | UART4. RXD_MUX | SDMA. DEBUG_PC[7] | GPIO5 [31] | MMDC_DEBUG[36] | CHEETAH. TRACE[10] |
| 176 | 32kout | ASRC_EXT_C LK | HDMI_TX_D DC_SDA | KEY_ROW3 | I2C2_SDA | GPIO4 [13] | SD1_VSELECT | |
| 177 | IPU1. CSIO_PIXCL OCK | | PCIE_CTRL. DIAG_STATU S_BUS_MUX [12] | | | GPIO5 [18] | | |

3.3. 40-pin FFC Connector Pin-out

| Pin # | Pin Name | Type | Pin Group | GPIO | i.MX6 Ball | Ball State |
|-------|------------|-------|-----------------------|-----------|------------|------------|
| 1 | JTAG_TDI | I | JTAG data-in | | G5 | - |
| 2 | EIM_A16 | IO | WEIM A16 signal | GPIO2[22] | H25 | PD |
| 3 | JTAG_NTRST | I | JTAG reset | | C2 | - |
| 4 | JTAG_TMS | I | JTAG test mode select | | C3 | - |
| 5 | JTAG_TCK | O | JTAG test clock | | H5 | - |
| 6 | EIM_A17 | IO | WEIM A17 signal | GPIO2[21] | G24 | PD |
| 7 | JTAG_TDO | O | JTAG data-out | | G6 | - |
| 8 | DGND | POWER | Digital GND | | | - |
| 9 | EIM_WAIT | IO | WEIM wait signal | GPIO5[0] | M25 | PD |
| 10 | EIM_A18 | IO | WEIM A18 signal | GPIO2[20] | J22 | PD |
| 11 | EIM_A24 | IO | WEIM A24 signal | GPIO5[4] | F25 | PD |
| 12 | EIM_CS0 | IO | WEIM CS0 signal | GPIO2[23] | H24 | - |
| 13 | EIM_CS1 | IO | WEIM CS1 signal | GPIO2[24] | J23 | - |
| 14 | EIM_A22 | IO | WEIM A22 signal | GPIO2[16] | F24 | PD |
| 15 | EIM_OE | IO | WEIM OE signal | GPIO2[25] | J24 | - |
| 16 | EIM_EB1 | IO | WEIM EB1 signal | GPIO2[29] | K23 | PD |
| 17 | EIM_DA3 | IO | WEIM DA3 signal | GPIO3[3] | K24 | PD |
| 18 | EIM_DA6 | IO | WEIM DA6 signal | GPIO3[6] | K25 | PU |
| 19 | EIM_DA1 | IO | WEIM DA1 signal | GPIO3[10] | J25 | PD |
| 20 | EIM_A20 | IO | WEIM A20 signal | GPIO2[18] | H22 | PD |
| 21 | EIM_DA5 | IO | WEIM DA5 signal | GPIO3[5] | L23 | PD |
| 22 | EIM_DA7 | IO | WEIM DA7 signal | GPIO3[7] | L25 | PU |
| 23 | EIM_DA8 | IO | WEIM DA8 signal | GPIO3[8] | L24 | PD |
| 24 | EIM_A19 | IO | WEIM A19 signal | GPIO2[19] | G25 | PD |
| 25 | EIM_LBA | IO | WEIM LBA signal | GPIO2[27] | K22 | PD |
| 26 | EIM_EB0 | IO | WEIM EB0 signal | GPIO2[28] | K21 | PD |
| 27 | EIM_DA12 | IO | WEIM DA12 signal | GPIO3[12] | M24 | PD |
| 28 | EIM_DA14 | IO | WEIM DA14 signal | GPIO3[14] | N23 | PD |
| 29 | EIM_BCLK | IO | WEIM BCLK signal | GPIO6[31] | N22 | - |
| 30 | EIM_DA0 | IO | WEIM DA0 signal | GPIO3[0] | L20 | PD |
| 31 | EIM_DA15 | IO | WEIM DA15 signal | GPIO3[15] | N24 | PD |
| 32 | EIM_DA2 | IO | WEIM DA2 signal | GPIO3[2] | L21 | PD |
| 33 | EIM_DA9 | IO | WEIM DA9 signal | GPIO3[9] | M21 | PD |
| 34 | EIM_DA4 | IO | WEIM DA4 signal | GPIO3[4] | L22 | PD |
| 35 | EIM_DA10 | IO | WEIM DA10 signal | GPIO3[10] | M22 | PD |
| 36 | DGND | POWER | Digital GND | | | - |

| Pin # | Pin Name | Type | Pin Group | GPIO | i.MX6 Ball | Ball State |
|-------|----------|------|------------------|-----------|------------|------------|
| 37 | EIM_DA13 | IO | WEIM DA13 signal | GPIO3[13] | M23 | PU |
| 38 | EIM_DA11 | IO | WEIM DA11 signal | GPIO3[11] | M20 | PU |
| 39 | EIM_A23 | IO | WEIM A23 signal | GPIO6[6] | J21 | PD |
| 40 | EIM_RW | IO | WEIM RW signal | GPIO2[26] | K20 | PD |

3.4. 40-pin FFC Mux

The table below summarizes the additional available functionality for each pin in the 40pin FFC connector.

| PIN | MODE 0 | MODE 1 | MODE 2 | MODE 3 | MODE 4 | MODE 5 | MODE 6 | MODE 7 |
|-----|--------------|---------------------|-------------------|------------------------------|------------------------------|-----------|----------------------------|----------------------|
| 1 | JTAG_TDI | | | | | | | |
| 2 | WEIM_A[16] | IPU1. DI1_DISP_CLK | IPU2. CSI1_PIXCLK | | MIPI_CORE. DPHY_TEST_OUT[23] | GPIO2[22] | TPSMP. HDATA[6] | SRC. BT_CFG[16] |
| 3 | JTAG_NTRST | | | | | | | |
| 4 | JTAG_TMS | | | | | | | |
| 5 | JTAG_TCK | | | | | | | |
| 6 | WEIM_A[17] | IPU1. DISP1_DAT[12] | IPU2. CSI1_D[12] | | MIPI_CORE. DPHY_TEST_OUT[22] | GPIO2[21] | TPSMP. HDATA[5] | SRC. BT_CFG[17] |
| 7 | JTAG_TDO | | | | | | | |
| 9 | WEIM_WA[IT] | WEIM_DTA[CK_B] | | | | GPIO5[0] | TPSMP. HDATA[30] | SRC. BT_CFG[25] |
| 10 | WEIM_A[18] | IPU1. DISP1_DAT[13] | IPU2. CSI1_D[13] | | MIPI_CORE. DPHY_TEST_OUT[21] | GPIO2[20] | TPSMP. HDATA[4] | SRC. BT_CFG[18] |
| 11 | WEIM_A[24] | IPU1. DISP1_DAT[19] | IPU2. CSI1_D[19] | IPU2. SISG[2] | IPU1. SISG[2] | GPIO5[4] | PL301_MX6Q_P[ER1. HPROT[2] | SRC. BT_CFG[24] EIM_ |
| 12 | WEIM_CS[0] | IPU1. DI1_PIN5 | ECSPI2. SCLK | | MIPI_CORE. DPHY_TEST_OUT[24] | GPIO2[23] | TPSMP. HDATA[7] | |
| 13 | WEIM_CS[1] | IPU1. DI1_PIN6 | ECSPI2. MOSI | | MIPI_CORE. DPHY_TEST_OUT[25] | GPIO2[24] | TPSMP. HDATA[8] | |
| 14 | WEIM_A[22] | IPU1. DISP1_DAT[17] | IPU2. CSI1_D[17] | | | GPIO2[16] | TPSMP. HDATA[0] | SRC. BT_CFG[22] |
| 15 | WEIM_OE | IPU1. DI1_PIN7 | ECSPI2. MISO | | MIPI_CORE. DPHY_TEST_OUT[26] | GPIO2[25] | TPSMP. HDATA[9] | |
| 16 | WEIM_EB[1] | IPU1. DISP1_DAT[10] | IPU2. CSI1_D[10] | MIPI_CORE. DPHY_TEST_OUT[1] | | GPIO2[29] | TPSMP. HDATA[13] | SRC. BT_CFG[28] |
| 17 | WEIM_DA_A[3] | IPU1. DISP1_DAT[6] | IPU2. CSI1_D[6] | MIPI_CORE. DPHY_TEST_OUT[5] | ANATOP. USBPHY1_TSTI_TX_HIZ | GPIO3[3] | TPSMP. HDATA[17] | SRC. BT_CFG[3] |
| 18 | WEIM_DA_A[6] | IPU1. DISP1_DAT[3] | IPU2. CSI1_D[3] | MIPI_CORE. DPHY_TEST_OUT[8] | ANATOP. USBPHY1_TSTI_TX_DN | GPIO3[6] | TPSMP. HDATA[20] | SRC. BT_CFG[6] |
| 19 | WEIM_DA_A[1] | | IPU2. CSI1_D[8] | | | GPIO3[1] | | |
| 20 | WEIM_A[20] | IPU1. DISP1_DAT[15] | IPU2. CSI1_D[15] | MIPI_CORE. DPHY_TEST_OUT[19] | | GPIO2[18] | TPSMP. HDATA[2] | SRC. BT_CFG[20] |
| 21 | WEIM_DA_A[5] | IPU1. DISP1_DAT[4] | IPU2. CSI1_D[4] | MIPI_CORE. DPHY_TEST_OUT[7] | ANATOP. USBPHY1_TSTI_TX_DP | GPIO3[5] | TPSMP. HDATA[19] | SRC. BT_CFG[5] |
| 22 | WEIM_DA_A[7] | IPU1. DISP1_DAT[2] | IPU2. CSI1_D[2] | MIPI_CORE. DPHY_TEST_OUT[9] | | GPIO3[7] | TPSMP. HDATA[21] | SRC. BT_CFG[7] |

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| PIN | MODE 0 | MODE 1 | MODE 2 | MODE 3 | MODE 4 | MODE 5 | MODE 6 | MODE 7 |
|-----|---------------|---------------------|--------------------|------------------------------|---------------------------------|-----------|--------------------------|------------------|
| 23 | WEIM_DA_A[8] | IPU1. DISP1_DAT[1] | IPU2. CSI1_D[1] | MIPI_CORE. DPHY_TEST_OUT[10] | | GPIO3[8] | TPSMP. HDATA[22] | SRC. BT_CFG[8] |
| 24 | WEIM_A[19] | IPU1. DISP1_DAT[14] | IPU2. CSI1_D[14] | MIPI_CORE. DPHY_TEST_OUT[20] | | GPIO2[19] | TPSMP. HDATA[3] | SRC. BT_CFG[19] |
| 25 | WEIM_LBA | IPU1. DI1_PIN17 | ECSP12. SS1 | | | GPIO2[27] | TPSMP. HDATA[11] | SRC. BT_CFG[26] |
| 26 | WEIM_EB[0] | IPU1. DISP1_DAT[11] | IPU2. CSI1_D[11] | MIPI_CORE. DPHY_TEST_OUT[0] | CCM. PMIC_RDY | GPIO2[28] | TPSMP. HDATA[12] | SRC. BT_CFG[27] |
| 27 | WEIM_DA_A[12] | IPU1. DI1_PIN3 | IPU2. CSI1_VSYNC | MIPI_CORE. DPHY_TEST_OUT[14] | SDMA. DEBUG_EVT_CHN_LINES[3] | GPIO3[12] | TPSMP. HDATA[26] | SRC. BT_CFG[12] |
| 28 | WEIM_DA_A[14] | IPU1. DI1_D1_CS | CCM. DIO_EXT_CLK | MIPI_CORE. DPHY_TEST_OUT[16] | SDMA. DEBUG_EVT_CHN_LINES[5] | GPIO3[14] | TPSMP. HDATA[28] | TPSMP. HDATA[28] |
| 29 | WEIM_BCLK | IPU1. DI1_PIN16 | | | | GPIO6[31] | TPSMP. HDATA[31] | |
| 30 | WEIM_DA_A[0] | IPU1. DISP1_DAT[9] | IPU2. CSI1_D[9] | MIPI_CORE. DPHY_TEST_OUT[2] | | GPIO3[0] | TPSMP. HDATA[14] | SRC. BT_CFG[0] |
| 31 | WEIM_DA_A[15] | IPU1. DI1_PIN1 | IPU1. DI1_PIN4 | MIPI_CORE. DPHY_TEST_OUT[17] | | GPIO3[15] | TPSMP. HDATA[29] | SRC. BT_CFG[15] |
| 32 | WEIM_DA_A[2] | IPU1. DISP1_DAT[7] | IPU2. CSI1_D[7] | MIPI_CORE. DPHY_TEST_OUT[4] | ANATOP. USBPHY1_TSTI_TX_HS_MODE | GPIO3[2] | TPSMP. HDATA[16] | SRC. BT_CFG[2] |
| 33 | WEIM_DA_A[9] | IPU1. DISP1_DAT[0] | IPU2. CSI1_D[0] | MIPI_CORE. DPHY_TEST_OUT[11] | | GPIO3[9] | TPSMP. HDATA[23] | SRC. BT_CFG[9] |
| 34 | WEIM_DA_A[4] | IPU1. DISP1_DAT[5] | IPU2. CSI1_D[5] | MIPI_CORE. DPHY_TEST_OUT[6] | ANATOP. USBPHY1_TSTI_TX_EN | GPIO3[4] | TPSMP. HDATA[18] | SRC. BT_CFG[4] |
| 35 | WEIM_DA_A[10] | IPU1. DI1_PIN15 | IPU2. CSI1_DATA_EN | MIPI_CORE. DPHY_TEST_OUT[12] | | GPIO3[10] | TPSMP. HDATA[24] | SRC. BT_CFG[10] |
| 37 | WEIM_DA_A[13] | IPU1. DI1_D0_CS | CCM. DI1_EXT_CLK | MIPI_CORE. DPHY_TEST_OUT[15] | SDMA. DEBUG_EVT_CHN_LINES[4] | GPIO3[13] | TPSMP. HDATA[27] | SRC. BT_CFG[13] |
| 38 | WEIM_DA_A[11] | IPU1. DI1_PIN2 | IPU2. CSI1_HSYNC | MIPI_CORE. DPHY_TEST_OUT[13] | SDMA. DEBUG_EVT_CHN_LINES[6] | GPIO3[11] | TPSMP. HDATA[25] | SRC. BT_CFG[11] |
| 39 | WEIM_A[23] | IPU1. DISP1_DAT[18] | IPU2. CSI1_D[18] | IPU2. SISG[3] | IPU1. SISG[3] | GPIO6[6] | PL301_MX6Q_PER1_HPROT[3] | SRC. BT_CFG[23] |
| 40 | WEIM_RW | IPU1. DI1_PIN8 | ECSP12. SSO | MIPI_CORE. DPHY_TEST_OUT[27] | | GPIO2[26] | TPSMP. HDATA[10] | SRC. BT_CFG[29] |

4. SOM's interfaces

4.1. Display Interfaces

4.1.1. Overview

The VAR-SOM-MX6 consists of the following display interfaces:

- Two LVDS channels, driven by the LDB; pixel clock up to 170 MHz
- One HDMI port (ver. 1.4) - driven by the HDMI transmitter: Pixel clock up to 266 MHz (gated by the IPU capabilities)
- One MIPI/DSI port - driven by the MIPI/DSI transmitter; two data lanes @ 1 GHz
- Each IPU has two display ports. Up to four external ports can be active at any given time (additional asynchronous data flows can be sent though the parallel ports and the MIPI/DSI port).

4.1.2 DSI

VAR-SOM-MX6 MIPI DSI Host Controller supports up to 2 D-PHY data lanes:

- Bidirectional communication and escape mode support through the data lane
- Programmable display resolutions, from 160 x 120(QQVGA) to 1024 x 768(XVGA)
- Multiple peripheral support capability, configurable virtual channels
- Video mode pixel formats, 16 bpp (5,6,5 RGB), 18 bpp (6,6,6,RGB) packed, 18 bpp (6,6,6,RGB) loosely, 24 bpp (8,8,8,RGB)

DSI signals:

| Signal | Pin # | Type | Description |
|-----------|-------|------|----------------------------------|
| DSI_CLK0M | 142 | ODS | Negative DSI clock differential |
| DSI_CLK0P | 140 | ODS | Positive DSI clock differential |
| DSI_D0M | 141 | ODS | Negative DSI data 0 differential |
| DSI_D0P | 143 | ODS | Positive DSI data 0 differential |
| DSI_D1M | 145 | ODS | Negative DSI data 1 differential |
| DSI_D1P | 147 | ODS | Positive DSI data 1 differential |

4.1.3 HDMI

The HDMI module provides an HDMI standard interface port to an HDMI 1.4 compliant display

HDMI Signals:

| Signal | Pin # | Type | Description |
|-------------|-------|------|-----------------------------------|
| HDMI_CLKM | 150 | ODS | Negative HDMI clock differential |
| HDMI_CLKP | 152 | ODS | Positive HDMI clock differential |
| HDMI_D0M | 157 | ODS | Negative HDMI data 0 differential |
| HDMI_D0P | 155 | ODS | Positive HDMI data 0 differential |
| HDMI_D1M | 148 | ODS | Negative HDMI data 1 differential |
| HDMI_D1P | 146 | ODS | Positive HDMI data 1 differential |
| HDMI_D2M | 153 | ODS | Negative HDMI data 2 differential |
| HDMI_D2P | 151 | ODS | Positive HDMI data 2 differential |
| HDMI_DDCCEC | 156 | IO | One wire bidirectional CEC |
| HDMI_HPD | 154 | I | Hot plug detect |

4.1.4 LVDS Interface

LVDS Display Bridge (LDB) will be used to connect the IPU (Image Processing Unit) to the External LVDS display interface.

There are 2 LVDS channels. These outputs are used to communicate RGB data and controls to external LCD displays.

The LVDS ports may be used as follows:

- Single channel output
- Dual channel output (one input source, two channel outputs for two displays)
- Split channel output (one input source, split to two channels on output)
- Separate two channel output (two input sources from IPU)

LVDS0 Signals:

| Signal | Pin # | Type | Description |
|-------------|-------|------|------------------------------|
| LVDS0_TX0_N | 161 | ODS | Negative data 0 differential |
| LVDS0_TX0_P | 163 | ODS | Positive data 0 differential |
| LVDS0_TX1_N | 160 | ODS | Negative data 1 differential |
| LVDS0_TX1_P | 162 | ODS | Positive data 1 differential |
| LVDS0_TX2_N | 164 | ODS | Negative data 2 differential |
| LVDS0_TX2_P | 166 | ODS | Positive data 2 differential |
| LVDS0_TX3_N | 165 | ODS | Negative data 3 differential |
| LVDS0_TX3_P | 167 | ODS | Positive data 3 differential |
| LVDS0_CLK_N | 168 | ODS | Negative clock differential |
| LVDS0_CLK_P | 170 | ODS | Positive clock differential |

Table 4-1 LVDS Signals

LVDS1 Signals:

| Signal | Pin # | Type | Description |
|-------------|-------|------|------------------------------|
| LVDS1_TX0_N | 184 | ODS | Negative data 0 differential |
| LVDS1_TX0_P | 186 | ODS | Positive data 0 differential |
| LVDS1_TX1_N | 188 | ODS | Negative data 1 differential |
| LVDS1_TX1_P | 190 | ODS | Positive data 1 differential |
| LVDS1_TX2_N | 192 | ODS | Negative data 2 differential |
| LVDS1_TX2_P | 194 | ODS | Positive data 2 differential |
| LVDS1_TX3_N | 183 | ODS | Negative data 3 differential |
| LVDS1_TX3_P | 181 | ODS | Positive data 3 differential |
| LVDS1_CLK_N | 180 | ODS | Negative clock differential |
| LVDS1_CLK_P | 182 | ODS | Positive clock differential |

4.2. Touch Panel

The VAR-SOM-MX6 features a 4-wire resistive touch panel interface:

- Compatible with 4-wire resistive touch screens
- Pen-detection and nIRQ generation
- Supports several schemes of measurement, averaging to filter noise

Touch-screen Controller Signals:

| Signal | Pin # | Type | Description |
|--------|-------|------|----------------------|
| TS_X- | 187 | AI | Touch screen X minus |
| TS_Y- | 193 | AI | Touch screen Y minus |
| TS_X+ | 189 | AI | Touch screen X plus |
| TS_Y+ | 191 | AI | Touch screen Y plus |

4.3. Camera Interfaces

4.3.1. MIPI CSI-2

The CSI-2 Host Controller is a digital core that implements all protocol functions defined in the MIPI CSI-2 specification, providing an interface between the system and the MIPI D-PHY, allowing communication with an MIPI CSI-2 compliant camera sensor.

The MIPI CSI-2 host controller supports the following features:

- Compliance with MIPI Alliance standard for camera serial interface 2 (CSI-2), version 1.00 29th November, 2005
- Optional support for Camera Control Interface (CCI) through the use of DesignWare Core (DW_apb_i2c)
- Interface with MIPI D-PHY following PHY Protocol Interface (PPI), as defined in MIPI Alliance Specification for D-PHY, version 1.00.00 14th May, 2009
- Supports up to 4 D-PHY Rx data lanes
- Dynamically configurable multi-lane merging

- Long and short packet decoding
- Timing accurate signaling of frame and line synchronization packets
- Support for several frame formats such as:
 - General frame or digital interlaced video with or without accurate sync timing
 - Data type (packet or frame level) and virtual channel interleaving
- 32-bit image data interface delivering data formatted as recommended in CSI-2 specification
- Supports all primary and secondary data formats:
 - RGB, YUV and RAW color space definitions
 - From 24-bit down to 6-bit per pixel
 - Generic or user-defined byte-based data types
 - Error detection and correction:
 - PHY level
 - Packet level
 - Line level
 - Frame level

MIPI CSI-2 signals:

| Signal | Pin # | Type | Description |
|-----------|-------|------|------------------------------------|
| CSI_CLK0M | 137 | IDS | Negative CSI-2 clock differential |
| CSI_CLK0P | 135 | IDS | Positive CSI-2 clock differential |
| CSI_D0M | 121 | IDS | Negative CSI-2 data 0 differential |
| CSI_D0P | 119 | IDS | Positive CSI-2 data 0 differential |
| CSI_D1M | 123 | IDS | Negative CSI-2 data 1 differential |
| CSI_D1P | 125 | IDS | Positive CSI-2 data 1 differential |
| CSI_D2M | 129 | IDS | Negative CSI-2 data 2 differential |
| CSI_D2P | 127 | IDS | Positive CSI-2 data 2 differential |
| CSI_D3M | 131 | IDS | Negative CSI-2 data 3 differential |
| CSI_D3P | 133 | IDS | Positive CSI-2 data 3 differential |

4.3.2. Parallel CSIx

Based on i.MX6 IPU, the VAR-SOM-MX6 supports two camera ports - each controlled by a CSI sub-block, providing a connection to image sensors and related devices.

CSI0 can implement 12bit CSI interface.

CSI0 Signals on 200 pin SO-DIMM connector:

| Signal | Pin # | Type | Description |
|--------------|-------|------|------------------------|
| CSI0_DAT8 | 87 | IO | Camera data line |
| CSI0_DAT9 | 88 | IO | Camera data line |
| CSI0_DAT10 | 85 | IO | Camera data line |
| CSI0_DAT11 | 83 | IO | Camera data line |
| CSI0_DAT12 | 124 | IO | Camera data line |
| CSI0_DAT13 | 175 | IO | Camera data line |
| CSI0_DAT14 | 171 | IO | Camera data line |
| CSI0_DAT15 | 115 | IO | Camera data line |
| CSI0_DAT16 | 173 | IO | Camera data line |
| CSI0_DAT17 | 117 | IO | Camera data line |
| CSI0_DAT18 | 113 | IO | Camera data line |
| CSI0_DAT19 | 96 | IO | Camera data line |
| CSI0_DATA_EN | 122 | IO | Camera data enable |
| CSI0_HSYNCH | 81 | IO | Camera horizontal sync |
| CSI0_PIXCLK | 177 | IO | Camera pixel clock |
| CSI0_VSYNC | 120 | IO | Camera vertical sync |

CSI1 Signals:

CSI1 can implement 20bit CSI interface.

CSI1 Signals that are exposed by the 40-pin FFC connector

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| Signal | Pin # | Type | Description |
|-------------------|-------|------|------------------------|
| IPU2.CSI1_D[0] | 33 | IO | Camera data 0 line |
| IPU2.CSI1_D[1] | 23 | IO | Camera data 1 line |
| IPU2.CSI1_D[2] | 22 | IO | Camera data 2 line |
| IPU2.CSI1_D[3] | 18 | IO | Camera data 3 line |
| IPU2.CSI1_D[4] | 21 | IO | Camera data 4 line |
| IPU2.CSI1_D[5] | 34 | IO | Camera data 5 line |
| IPU2.CSI1_D[6] | 17 | IO | Camera data 6 line |
| IPU2.CSI1_D[7] | 32 | IO | Camera data 7 line |
| IPU2.CSI1_D[8] | 19 | IO | Camera data 8 line |
| IPU2.CSI1_D[9] | 30 | IO | Camera data 9 line |
| IPU2.CSI1_D[10] | 16 | IO | Camera data 10 line |
| IPU2.CSI1_D[11] | 26 | IO | Camera data 11 line |
| IPU2.CSI1_D[12] | 6 | IO | Camera data 12 line |
| IPU2.CSI1_D[13] | 10 | IO | Camera data 13 line |
| IPU2.CSI1_D[14] | 24 | IO | Camera data 14 line |
| IPU2.CSI1_D[15] | 20 | IO | Camera data 15 line |
| IPU2.CSI1_D[17] | 14 | IO | Camera data 17 line |
| IPU2.CSI1_D[18] | 39 | IO | Camera data 18 line |
| IPU2.CSI1_D[19] | 11 | IO | Camera data 19 line |
| IPU2.CSI1_DATA_EN | 35 | IO | Camera data enable |
| IPU2.CSI1_HSYNC | 38 | IO | Camera horizontal sync |
| IPU2.CSI1_PIXCLK | 2 | IO | Camera pixel clock |
| IPU2.CSI1_VSYNC | 27 | IO | Camera vertical sync |

CSI1 Signals that are exposed by the 200-pin connector

| | | | |
|-----------------|----|----|---------------------|
| IPU2.CSI1_D[16] | 86 | IO | Camera data 16 line |
|-----------------|----|----|---------------------|

4.4. Gigabit Ethernet

Gigabit Ethernet Features:

The Ethernet Media Access Controller (MAC) is designed to support 10/100/1000 Mbps Ethernet/IEEE 802.3 networks. An external Gigabit magnetics is required to complete the interface to the media. The i.MX6 processor also consists of HW assist for IEEE1588 standard. See the IEEE1588 section for more details.

Gigabit Ethernet Magnetics:

In order to utilize the VAR-SOM-MX6 Gigabit Ethernet interface, compatible magnetics should be used on the carrier board.

| Vendor | Part Number | Package | Cores | Configuration |
|--------|-------------|-----------------|-------|---------------|
| Pulse | H5007NL | Transformer | 8 | Auto-MDX |
| TDK | TLA-7T101LF | Transformer | 8 | Auto-MDX |
| Pulse | J0G-0009NL | Integrated RJ45 | 8 | Auto-MDX |

Gigabit Ethernet Signals:

| Signal | Pin # | Type | Description |
|--------|-------|------|------------------------------|
| MDI_A+ | 3 | DS | Positive A differential lane |
| MDI_A- | 5 | DS | Negative A differential lane |
| MDI_B+ | 9 | DS | Positive B differential lane |
| MDI_B- | 11 | DS | Negative B differential lane |
| MDI_C+ | 4 | DS | Positive C differential lane |
| MDI_C- | 6 | DS | Negative C differential lane |
| MDI_D+ | 10 | DS | Positive D differential lane |
| MDI_D- | 12 | DS | Negative D differential lane |

4.5. Wi-Fi & Bluetooth

The VAR-SOM-MX6 contains the LS Research TiWi-BLE, a high performance 2.4 GHz IEEE 802.11 b/g/n Bluetooth 4.0 radio module. The module is based on TI's WL-1271L chipset. The module realizes the necessary PHY/MAC layers to support WLAN applications in conjunction with a host processor over a SDIO interface.

The module also provides a Bluetooth platform through the HCI transport layer. Both WLAN and Bluetooth share the same antenna port.

- IEEE 802.11 b/g/n
- Bluetooth 4.0
- U.FL connector for external antenna.
- Integrated band-pass filter

4.6. USB Host 2.0

The USB controller block provides high performance USB functionality that conforms to the USB 2.0 specification.

USB Host1 Signals:

| Signal | Pin # | Type | Description |
|-------------|-------|------|---|
| USB_HOST_DP | 110 | IODS | Positive USB host data |
| USB_HOST_DN | 108 | IODS | Negative USB host data |
| USB_H1_VBUS | 104 | I | USB 2.0 VBUS indicator (5V) |
| USB_H1_OC | 79 | I | USB host over current indicator , Active low 3.3v digital |

4.7. USB 2.0 OTG

USB 2.0 On-the-go Features:

High-speed OTG core

- HS/FS/LS UTMI compliant interface
- High speed, full speed and low speed operation in host mode (with UTMI transceiver)
- High speed, and full speed operation in peripheral mode (with UTMI transceiver)
- Hardware support for OTG signaling, session request protocol, and host negotiation protocol
- Up to 8 bidirectional endpoints
- Integrated HS USB PHY

OTG Signals:

| Signal | Pin # | Type | Description |
|--------------|-------|------|---|
| USB_OTG_DN | 114 | IODS | Negative USB OTG data |
| USB_OTG_DP | 116 | IODS | Positive USB OTG data |
| USB_OTG_VBUS | 106 | I | USB 2.0 OTG VBUS indicator (5V) |
| USB_OTG_ID | 94 | I | USB OTG host/client ID Low : Host mode Float: Client mode |

4.8. MMC/SD/SDIO

MX6 MMC interface features:

- Fully compliant with MMC command/response sets and physical layer as defined in the Multimedia Card System specification v4.2/4.3/4.4, including high-capacity (size > 2 GB) cards HC MMC.
- Fully compliant with SD command/response sets and physical layer as defined in the SD Memory Card specifications v3.0, including high-capacity SDHC cards up to 32 GB
- Fully compliant with SDIO command/response sets and interrupt/read-wait mode as defined in the SDIO Card specification, Part E1 v1.10
- Fully compliant with SD Card specification, Part A2, SD Host Controller Standard specification v2.00
- 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to UHS-I SDR104 mode (104 MB/s max)

- 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards up to 52 MHz in both SDR and DDR modes (104 MB/s max). However, the SoC level integration and I/O muxing logic restrict functionality to the following:

SDMMC1 Signals:

| Signal | Pin # | Type | Description |
|-----------|-------|------|--|
| SD1_CLK | 72 | O | Clock for MMC/SD/SDIO card |
| SD1_CMD | 69 | IO | CMD line connect to card |
| SD1_DATA0 | 68 | IO | DAT0 line in all modes Also used to detect busy state |
| SD1_DATA1 | 71 | IO | DAT1 line-in |
| SD1_DATA2 | 70 | IO | DAT2 line |
| SD1_DATA3 | 73 | IO | DAT3 line-in |

SDMMC2 Signals:

| Signal | Pin # | Type | Description |
|-----------|-------|------|--|
| SD2_CLK | 60 | O | Clock for MMC/SD/SDIO card |
| SD2_CMD | 64 | IO | CMD line connect to card |
| SD2_DATA0 | 62 | IO | DAT0 line in all modes (also used to detect busy state) |
| SD2_DATA1 | 63 | IO | DAT1 line-in |
| SD2_DATA2 | 61 | IO | DAT2 line |
| SD2_DATA3 | 65 | IO | DAT3 line-in |

4.9. Audio

The VAR-SOM-MX6 features three audio interfaces:

- TLV320AIC3106 Audio codec interfaces
 1. Analog outputs / inputs:
 - stereo line-in
 - Stereo HP out
 2. Digital microphone input
- SSI Digital audio interface
- S/PDIF in/out

Analog audio signals are featured by the on-SOM TLV320AIC3106 audio codec. Refer to the data sheet for detailed electrical characteristics of the relevant interfaces

<http://www.ti.com/product/tlv320aic3106>.

AUDMUX4 Signals:

| Signal | Pin # | Type | Description |
|------------|-------|------|------------------------|
| HP_LOUT | 198 | AO | Headphones out - left |
| HP_ROUT | 200 | AO | Headphones out - right |
| LINEIN1_LP | 197 | AI | Line-in - Right |
| LINEIN1_RP | 199 | AI | Line-in - Left |

Digital AUDMUX:

Key features of the block include:

- Full 6-wire SSI interfaces for asynchronous receive and transmit
- Configurable 4-wire (synchronous) or 6-wire (asynchronous) peripheral interfaces
- Independent Tx/Rx frame sync and clock direction selection for host or peripheral
- Each host interface's capability to connect to any other host or peripheral interface in a point-to-point or point-to-multipoint (network mode)
- Transmit and receive data switching to support external network mode

AUDMUX4 Signals:

| Signal | Pin # | Type | Description |
|--------------|-------|------|---|
| AUDMUX4_TXD | 26 | IO | Transmit data from pin |
| AUDMUX4_RXD | 21 | IO | Receive data at pin |
| AUDMUX4_TXC | 25 | IO | Transmit clock input/output at pin |
| AUDMUX4_RXC | 22 | IO | Receive clock input/output at pin |
| AUDMUX4_TXFS | 24 | IO | Transmit frame sync input/output at pin |
| AUDMUX4_RXFS | 23 | IO | Receive frame sync input/output at pin |

S/PDIF (Sony Phillips Digital Interface) In/Out:

S/PDIF is a standard audio file transfer format, developed jointly by the Sony and Phillips corporations.

SPIDF Signals:

| Signal | Pin # | Type | Description |
|-------------|-----------|------|-------------|
| SPDIFIN | 75 | | In |
| SPDIFOUT | 77 | | Out |
| Spdif.plock | 44(MUXED) | | |
| Spdif.srclk | 46(MUXED) | | Clock |

4.10. UART Interfaces

By default four UART interfaces are supported, refer to Table 3.2 for further configurations the UART interface.

UART Features:

Each of the UART modules support the following serial data transmit/receive protocols and configurations:

- 7or 8-bit data words, one or two stop bits, programmable parity (even, odd or none)
- Programmable baud rates up to 4 MHz This is a higher max baud rate relative to the 1.875 MHz, which is stated by the TIA/EIA-232-F standard and the i.MX31 UART modules.
- 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud
- IrDA 1.0 support (up to SIR speed of 115200 bps)

UART1 Signals:

| Signal | Pin # | Type | Description |
|-----------|-------|------|--------------------------|
| UART1_CTS | 86 | O | UART HW flow control RTS |
| UART1_RTS | 84 | I | UART HW flow control CTS |
| UART1_TX | 85 | O | UART transmit |
| UART1_RX | 83 | I | UART receive |

Note: UART1 is used as default boot debug port.

UART2 Signals:

| Signal | Pin # | Type | Description |
|-----------|-------|------|--------------------------|
| UART2_TXD | 52 | O | UART transmit |
| UART2_RXD | 53 | I | UART receive |
| UART2_RTS | 51 | I | UART HW flow control RTS |
| UART2_CTS | 50 | O | UART HW flow control CTS |

Note: UART2 Signals are shared with the on-som Bluetooth.

UART3 Signals:

| Signal | Pin # | Type | Description |
|--------------------------|-------|------|--------------------------|
| UART3_TXD | 56 | O | UART transmit |
| UART3_RXD | 54 | I | UART receive |
| UART3_RTS ^[1] | 57 | I | UART HW flow control RTS |
| UART3_CTS | 55 | O | UART HW flow control CTS |

[1] UART3 RTS pin is being latched at boot to determine boot sequence. Use with OE# buffer, and enable only after SOM is powered-up. Use reference schematics as example.

UART5 Signals:

| Signal | Pin # | Type | Description |
|-----------|-------|------|--------------------------|
| UART5_TXD | 41 | O | UART transmit |
| UART5_RXD | 39 | I | UART receive |
| UART5_RTS | 80 | I | UART HW flow control RTS |
| UART5_CTS | 82 | O | UART HW flow control CTS |

4.11. Flexible Controller Area Network (FLEXCAN)

The CAN protocol was primarily, but not exclusively, designed to be used as a vehicle serial data bus, meeting the specific requirements of this field: Real-time processing, reliable operation in the Electromagnetic Interference (EMI) environment of a vehicle, cost-effectiveness and required bandwidth. The FlexCAN module is a full implementation of the CAN protocol specification, version 2.0 B, which supports both standard and extended message frames.

CAN1 Signals:

| Signal | Pin # | Type | Description |
|---------|-------|------|------------------|
| CAN1_RX | 46 | I | CAN BUS receive |
| CAN1_TX | 44 | O | CAN BUS transmit |

CAN2 Signals:

| Signal | Pin # | Type | Description |
|---------|-------|------|------------------|
| CAN2_TX | 80 | O | CAN BUS receive |
| CAN2_RX | 82 | I | CAN BUS transmit |

Signal Descriptions

CAN Rx: The receive pin from the CAN bus transceiver. Dominant state is represented by logic level '0'. Recessive state is represented by logic level '1'.

CAN Tx: The transmit pin to the CAN bus transceiver. Dominant state is represented by logic level '0'. Recessive state is represented by logic level '1'.

4.12. SPI

The Enhanced Configurable Serial Peripheral Interface (ECSPI) is a full-duplex, synchronous 4-wire serial communication block. The ECSPI contains a 64 x 32 receive buffer (RXFIFO) and a 64 x 32 transmit buffer (TXFIFO). With data FIFOs, the ECSPI allows rapid data communication with fewer software interruptions.

4.12.1. eCSPI Key Features:

- Full-duplex synchronous serial interface
- Master/slave configurable
- Four chip select (SS) signals to support multiple peripherals
- Transfer continuation function allows unlimited length data transfers
- 32-bit wide by 64-entry FIFO for both transmitting and receiving data
- 32-bit wide by 16-entry FIFO for HT message data
- Polarity and phase of the chip select (SS) and SPI clock (SCLK) are configurable
- Direct Memory Access (DMA) support
- Max operation frequency up to the reference clock frequency

ECSPI1 Signals:

| Signal | Pin # | Type | Description |
|------------|---------|------|---------------------------|
| cSPI1_CLK | 25, 43 | IO | SPI1 clock |
| cSPI1_MOSI | 26, 45 | IO | SPI1 MOSI signal |
| cSPI1_MISO | 24, 41 | IO | SPI1 SOMI signal |
| cSPI1_CS0 | 39, 56 | IO | SPI1 chip select 0 signal |
| cSPI1_CS1 | 48, 86 | IO | SPI1 chip select 1 signal |
| cSPI1_CS2 | 52 | IO | SPI1 chip select 2 signal |
| cSPI1_CS3 | 54, 174 | IO | SPI1 chip select 3 signal |

ECSPI2 Signals:

| Signal | Pin # | Type | Description |
|------------|--------|------|---------------------------|
| cSPI2_CLK | 22, 87 | IO | SPI2 clock |
| cSPI2_MOSI | 88 | IO | SPI2 MOSI signal |
| cSPI2_MISO | 85 | IO | SPI2 SOMI signal |
| cSPI2_CS0 | 23, 83 | IO | SPI2 Chip select 0 signal |
| cSPI2_CS2 | 52 | IO | SPI2 Chip select 2 signal |
| cSPI2_CS3 | 54 | IO | SPI2 Chip select 3 signal |

ECSPI4 Signals:

| Signal | Pin # | Type | Description |
|------------|--------|------|---------------------------|
| cSPI4_CLK | 75 | IO | SPI4 clock |
| cSPI4_MOSI | 50 | IO | SPI4 MOSI signal |
| cSPI4_MISO | 77 | IO | SPI4 SOMI signal |
| cSPI4_CS0 | 51, 84 | IO | SPI4 Chip select 0 signal |
| cSPI4_CS2 | 52 | IO | SPI4 Chip select 2 signal |
| cSPI4_CS3 | 54 | IO | SPI4 Chip select 3 signal |
| cSPI4_RDY | 57 | IO | SPI4 ready signal |

4.13. PCIe

VAR-SOM-MX6 PCI Express functionality has the following parts:

PCI Express includes the following cores:

- PCI Express Dual Mode (DM) core
- PCI Express Root Complex (RC) core
- PCI Express Endpoint (EP) core

PCI Express 2.0 PHY:

- PCIe 2.0 PHY is a complete mixed-signal semiconductor intellectual property (IP) solution, designed for single-chip integration into computer applications
- The PCIe 2.0 PHY supports both the 5 Gbps data rate of the PCI Express Gen 2.0 specifications as well as being backwards compatible to the 2.5Gb/s Gen 1.1 specification

PCIE Signals:

| Signal | Pin # | Type | Description |
|----------|-------|------|---------------------------------|
| PCIE_TXP | 130 | DS | Positive PCI TX differential |
| PCIE_TXM | 128 | DS | Negative PCI TX differential |
| PCIE_RXP | 134 | DS | Positive PCI RX differential |
| PCIE_RXM | 136 | DS | Negative PCI RX differential |
| CLK1_P | 102 | DS | Positive PCI clock differential |
| CLK1_N | 100 | DS | Negative PCI clock differential |

4.14. Serial ATA

VAR-SOM-MX6 includes an integrated Serial Advanced Technology Attachment (SATA) controller that is compatible with the Advanced Host Controller Interface (AHCI) specification.

The SATA Controller block (SATA) along with integrated physical link hardware (SATA PHY) provide one SATA port for the attachment of external SATA compliant storage devices.

SATA Signals:

| Signal | Pin # | Type | Description |
|----------|-------|------|-------------------------------|
| SATA_RXN | 91 | DS | Negative SATA RX differential |
| SATA_RXP | 93 | DS | Positive SATA RX differential |
| SATA_TXN | 99 | DS | Negative SATA TX differential |
| SATA_TXP | 97 | DS | Positive SATA TX differential |

4.15. I²C

I2C-1, 2, 3 Interface connectivity peripherals provide serial interface for external devices. Data rates of up to 400 kbps are supported.

I2C1 Signals:

| Signal | Pin # | Type | Description |
|----------|-------|------|---|
| I2C1_SCL | 88,75 | IO | I2C1 I ² C clock, open drain |
| I2C1_SDA | 87,50 | IO | I2C1 I ² C data, open drain |

I2C2 Signals:

| Signal | Pin # | Type | Description |
|----------|-------|------|---|
| I2C2_SCL | 174 | IO | I ² C clock, open drain, internally PU |
| I2C2_SDA | 176 | IO | I ² C data, open drain, internally PU |

Note: I2C2 interface is used by PMIC & CODEC on-som devices (I2C ADDR =0x1B,0x8). Pin configuration for I2C2 signal can't be changed.

I2C3 Signals:

| Signal | Pin # | Type | Description |
|----------|-------|------|---|
| I2C3_SCL | 92 | IO | I2C3 I ² C clock, open drain |
| I2C3_SDA | 90 | IO | I2C3 I ² C data, open drain |

4.16. Local Bus

The EIM handles the interface to devices external to the chip, including generation of chip selects, clock and control for external peripherals and memory. It provides asynchronous access to devices with a SRAM-like interface and synchronous access to devices with Nor-Flash-like or PSRAM-like interfaces.

The local bus signals are split between two connectors: SODIMM 200 connector and 40-pin FFC connector.

Local Bus Signals on SODIMM Connector:

| Signal | Pin # | Type | Description |
|---------------|-------|------|-------------------------|
| WEIM_D[19] | 86 | IO | Local Bus D[19] signal |
| WEIM_D[20] | 84 | IO | Local Bus D[20] signal |
| WEIM_D[21] | 75 | IO | Local Bus D[21] signal |
| WEIM_D[22] | 77 | IO | Local Bus D[22] signal |
| WEIM_D[23] | 55 | IO | Local Bus D[23] signal |
| WEIM_D[26] | 52 | IO | Local Bus D[24] signal |
| WEIM_D[25] | 54 | IO | Local Bus D[25] signal |
| WEIM_D[27] | 53 | IO | Local Bus D[27] signal |
| WEIM_D[28] | 50 | IO | Local Bus D[28] signal |
| WEIM_D[29] | 51 | IO | Local Bus D[29] signal |
| WEIM_D[30] | 79 | IO | Local Bus D[30] signal |
| WEIM_DA_A[13] | 40 | IO | Local Bus DA[13] signal |
| WEIM_D[24] | 56 | IO | Local Bus EB[2] signal |
| WEIM_EB[3] | 57 | IO | Local Bus EB[3] signal |
| WEIM_D[8] | 124 | IO | Local Bus D[8] signal |
| WEIM_D[9] | 175 | IO | Local Bus D[9] signal |
| WEIM_D[10] | 171 | IO | Local Bus D[10] signal |
| WEIM_D[11] | 115 | IO | Local Bus D[11] signal |
| WEIM_D[12] | 173 | IO | Local Bus D[12] signal |
| WEIM_D[13] | 117 | IO | Local Bus D[13] signal |
| WEIM_D[14] | 113 | IO | Local Bus D[14] signal |
| WEIM_D[15] | 96 | IO | Local Bus D[15] signal |
| WEIM_D[6] | 87 | IO | Local Bus D[6] signal |
| WEIM_D[7] | 88 | IO | Local Bus D[7] signal |
| WEIM_D[0] | 122 | IO | Local Bus D[0] signal |
| WEIM_D[1] | 120 | IO | Local Bus D[1] signal |
| WEIM_CS[2] | 63 | IO | Local Bus CS[2] signal |
| WEIM_CS[3] | 61 | IO | Local Bus CS[3] signal |
| WEIM_CS[2] | 23 | IO | Local Bus CS[2] signal |
| WEIM_CS[3] | 22 | IO | Local Bus CS[3] signal |
| WEIM_DA_A[7] | 42 | IO | Local Bus DA[7] signal |
| WEIM_DA_A[13] | 37 | IO | Local Bus DA[13] signal |

Local Bus Signals 40 Pin FFC connector:

| Signal | Pin # | Type | Description |
|------------|-------|------|------------------------|
| WEIM_A[16] | 2 | IO | Local Bus A[16] signal |
| WEIM_A[17] | 6 | IO | Local Bus A[17] signal |
| WEIM_WAIT | 9 | IO | Local Bus Wait signal |
| WEIM_A[18] | 10 | IO | Local Bus A[18] signal |
| WEIM_A[24] | 11 | IO | Local Bus A[24] signal |
| WEIM_CS[0] | 12 | IO | Local Bus CS[0] signal |
| WEIM_CS[1] | 13 | IO | Local Bus CS[1] signal |

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| Signal | Pin # | Type | Description |
|---------------|-------|------|-------------------------|
| WEIM_A[22] | 14 | IO | Local Bus A[22] signal |
| WEIM_OE | 15 | IO | Local Bus OE signal |
| WEIM_EB[1] | 16 | IO | Local Bus EB[1] signal |
| WEIM_DA_A[3] | 17 | IO | Local Bus DA[3] signal |
| WEIM_DA_A[6] | 18 | IO | Local Bus DA[6] signal |
| WEIM_DA_A[1] | 19 | IO | Local Bus DA[10] signal |
| WEIM_A[20] | 20 | IO | Local Bus A[20] signal |
| WEIM_DA_A[5] | 21 | IO | Local Bus DA[5] signal |
| WEIM_DA_A[8] | 23 | IO | Local Bus DA[8] signal |
| WEIM_A[19] | 24 | IO | Local Bus A[19] signal |
| WEIM_LBA | 25 | IO | Local Bus LBA signal |
| WEIM_EB[0] | 26 | IO | Local Bus EB[0] signal |
| WEIM_DA_A[12] | 27 | IO | Local Bus DA[12] signal |
| WEIM_DA_A[14] | 28 | IO | Local Bus DA[14] signal |
| WEIM_BCLK | 29 | IO | Local Bus BCLK signal |
| WEIM_DA_A[0] | 30 | IO | Local Bus DA[0] signal |
| WEIM_DA_A[15] | 31 | IO | Local Bus DA[15] signal |
| WEIM_DA_A[2] | 32 | IO | Local Bus DA[2] signal |
| WEIM_DA_A[9] | 33 | IO | Local Bus DA[9] signal |
| WEIM_DA_A[4] | 34 | IO | Local Bus DA[4] signal |
| WEIM_DA_A[10] | 35 | IO | Local Bus DA[10] signal |
| WEIM_DA_A[11] | 38 | IO | Local Bus DA[11] signal |
| WEIM_A[23] | 39 | IO | Local Bus A[23] signal |
| WEIM_RW | 40 | IO | Local Bus RW signal |

4.17. JTAG

The System JTAG Controller (SJC) provides debug and test control with maximum security. The test access port (TAP) is designed to support features compatible with the IEEE standard 1149.1 v2001 (JTAG). Support IEEE P1149.6 extensions to the JTAG standard are for AC testing of selected IO signals.

JTAG signals 40-pin FFC Connector:

| Signal | Pin # | Type | Description |
|------------|-------|------|-----------------------|
| JTAG_TDI | 1 | I | JTAG data-in |
| JTAG_NTRST | 3 | I | JTAG reset |
| JTAG_TMS | 4 | I | JTAG test mode select |
| JTAG_TCK | 5 | O | JTAG test clock |
| JTAG_TDO | 7 | O | JTAG data-out |

4.18. General Purpose IOs

Most of the SoM's IO pins can be used as GPIOs. See Chapter 3, Table 3.1 and 3.2 for a complete SoM connectors signal list and GPIO multiplexing.

4.19. General System Control

4.19.1. Boot Options

Below you can find the MX6 boot options

| 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
|---------------------------------|-----------|-----------|-----------|--|-----------|---|-----------|
| BT_CFG1_7 | BT_CFG1_6 | BT_CFG1_5 | BT_CFG1_4 | BT_CFG2_6 | BT_CFG2_5 | BT_CFG2_4 | BT_CFG2_3 |
| 1XXX = NANDF Boot | | | | | | | |
| 011X = MMC/eMMC Boot | | | | X0 = 1-bit X1 = 4-bit 10 = 8-bit | | 01 = SD2 Boot 10 = SD3 Boot 11 = SD4 Boot | |
| 010X = SD/eSD Boot | | | | X0 = 1-bit X1 = 4-bit | | 01 = SD2 Boot 10 = SD3 Boot 11 = SD4 Boot | |
| 0011 = Serial ROM (SPINOR) Boot | | | | | | | |
| 0010 = SATA Boot | | | | | | | |

The boot-select pin configures the boot sequence of the VAR-SOM-MX6:

BOOT_CFG = X1000X01

| Pin Name | Pin Number | MX6 BOOT_CFG | Internally pulled |
|-----------|------------|--------------|-------------------|
| BOOT_SEL0 | 42 | BT_CFG1_7 | PULLED UP 10K |
| BOOT_SEL1 | 40 | BT_CFG2_5 | PULLED UP 10K |

Use cases:

BOOT_SEL [1:0] = [0:1] => BOOT_CFG = 11000X01 => NAND Boot

BOOT_SEL [1:0] = [1:0] => BOOT_CFG = 01000101 => SD2 boot, 4 bit bus

4.19.2. Reset

'0' logic will reset VAR-SOM-MX6

4.19.3. Reference Clock Out

VAR-SOM-MX6 output clock (CLKO2) is controlled by the i.MX6 CCM module. Please refer to the i.MX6 user manual regarding the configuration option for this clock.

4.19.4. General System Control Signals

| Signal | Pin # | Type | Description |
|-----------|-------|------|--|
| CLKO | 29 | O | Clock out |
| BOOT_SELO | 42 | I | System boot option select [high – NAND boot] |
| BOOT_SEL1 | 40 | I | Pull-up or leave N.C |
| POR_B | 98 | I | Hardware reset |

4.20. Power

4.20.1. Power Supply

| Signal | Pin # | Type | Description |
|---------|--|-----------|--|
| VIN_3V3 | 32, 34, 36, 38, 103, 105, 107, 109, 111 | Power In | VAR-SOM-OMX6 Single DC-IN Supply voltage. Voltage range: 3.3 +/- 5% |
| 3V3_PER | 49 | Power Out | 3.3 V output, up to 200 mA |

4.20.2. Ground

| Signal | Pin # | Type | Description |
|--------|---|-------|----------------|
| GND | 13, 14, 19, 27, 28, 31, 33, 35, 37, 47, 58, 59, 66, 67, 76, 78, 89, 95, 101, 112, 118, 126, 132, 138, 139, 144, 149, 158, 159, 169, 172, 178, 179, 185 | Power | Digital ground |
| AGND | 195,196 | Power | Analog GND |

5. Absolute Maximum Characteristics

| Power Supply | Min | Max | Unit |
|--------------------------|------|-----|------|
| Main Power Supply, DC-IN | -0.3 | 3.5 | V |

6. Operational Characteristics

6.1. Power supplies

| | Min | Typical | Max | Unit |
|--------------------------|-----|---------|-----|------|
| Main Power Supply, DC-IN | -5% | 3.3 | +5% | V |

6.2. Power Consumption

CPU usage:

| Task | SOM VBAT current draw in ma @3.3v |
|-------------------------------------|-----------------------------------|
| Idle (~10% CPU) @ 400mhz | 330mA |
| FHD Video playback | 530ma |
| 100% CPU Dhrystone test – Dual core | 630ma |
| 100% CPU Dhrystone test – Quad core | 900ma |

Additional peripherals:

| Task | SOM VBAT current draw in ma @3.3v |
|-------------------|-----------------------------------|
| WLAN transmission | 200mA |
| Gbit Ethernet | 150ma |

7. DC Electrical Characteristics

| Parameter | Min | Typical | Max | Unit |
|-----------------|---------------|---------|--------------|------|
| Digital 3.3V | | | | |
| V _{IH} | 0.7x VIN_3V3 | | VIN_3V3 | V |
| V _{IL} | 0 | | 0.3x VIN_3V3 | V |
| V _{OH} | VIN_3V3- 0.15 | | | V |
| V _{OL} | | | 0.15 | V |

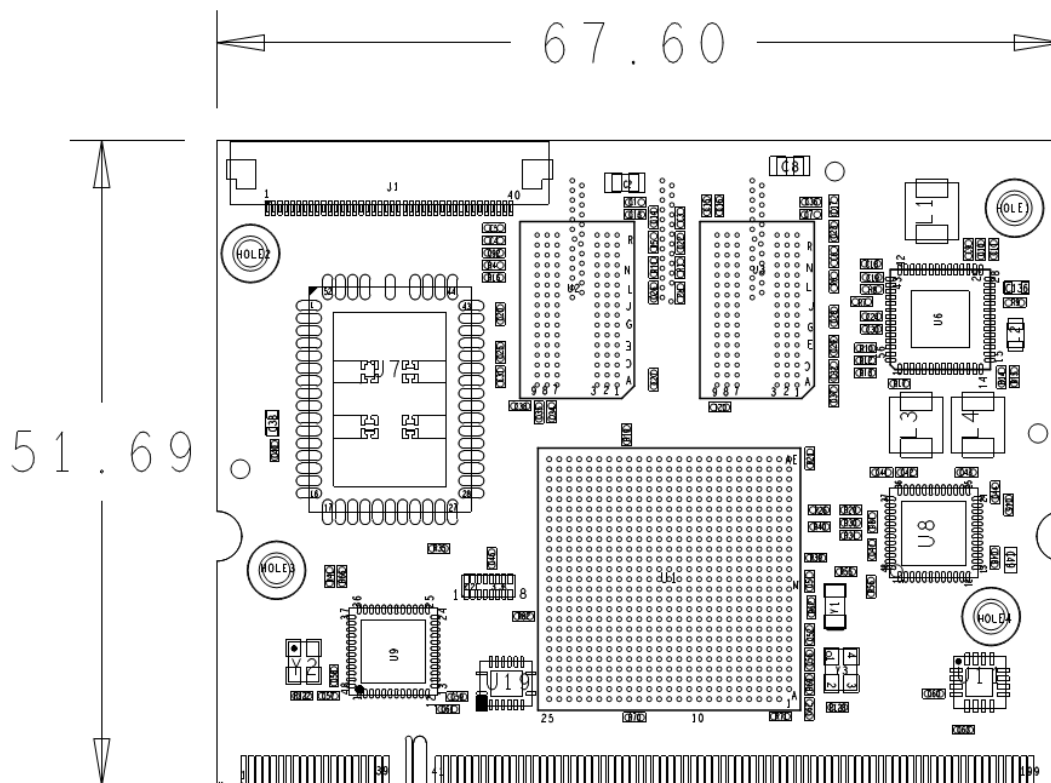
Table 7-1 DC Electrical Characteristics

8. Environmental Specifications

| | Min | Max |
|---|----------------|--------|
| Commercial Operating Temperature Range | 0 °C | +70 °C |
| Extended Operating Temperature Range | -25 °C | +70 °C |
| Industrial Operating Temperature Range | -40 °C | +85 °C |
| Referring MIL-HDBK-217F-2 Parts Count Reliability Prediction Method Model: 50Deg Celsius, Class B-1, GM | 121 Khrs > | |
| 50Deg Celsius, Class B-1, GB | 1400 Khrs > | |
| Shock Resistance | 50G/20 ms | |
| Vibration | 20G/0 - 600 Hz | |

9. Mechanical Drawings

Top View [mm]



CAD files are available for download at <http://www.variscite.com/>

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