VARISCITE LTD.

VAR-SOM-SOLO/DUAL v1.X Datasheet

Freescale i.MX6™ - based System-on-Module

VARISCITE LTD.

VAR-SOM-SOLO/DUAL Datasheet

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Document Revision History

Revision	Date	Notes
1.0	09/9/2014	Initial
1.01	25/12/2014	Section 3.2 – Updated: pins 16, 94, removed pin 70 Section 8 - Updated Section 9 - Updated
1.02	02/06/2015	Updated -MIPI CSI-2 supporting 2 lanes Section 3.1 - Pins 127,129,131,133 N.C. Section 4.3.1 - Pins 127,129,131,133 Removed
1.03	07/07/2015	Section 4.3.2 - Removed CSI1 Table
1.04	11/01/2016	Section 3.1 - Updated Note [2] Section 4.10 - Corrected UART number, updated note Section 4.14 - Updated note
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1.09	02/11/2017	Section 1.2, 2.5, 4.5 – Updated Bluetooth features
1.10	21/12/2017	Section 3.1, 4.10 – Updated UART features, notes, pinmux tables
1.11	22/01/2018	Section 3.2 – Updated pins 42,60 68-73
1.12	25/07/2018	Section 8 – Updated Reliability prediction data
1.13	31/10/2018	Section 3.2 – Updated pins 71-73
1.14	20/11/2018	Section 3.1 – Added note [5] Section 3.2 – corrected typos, added alt modes 8,9
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1.16	20/10/2020	Section 1.3 – Updated Block Diagram
1.17	20/03/2022	Added Ethernet PHY ADIN1300 – Updated section 2.3
1.18	02/05/2022	Section 8 – Updated table
1.19	17/05/2022	Sections: 1.2,2.5,4.5 – Updated the BT
1.20	27/02/2023	Section 8 – Updated table Sections 1.2, 2.2 – Updated the eMMC

1. Overview

1.1. General Information

The VAR-SOM-SOLO/DUAL is a high performance System-on-Module. It provides an ideal building block that easily integrates with a wide range of target markets requiring rich multimedia functionality, powerful graphics and video capabilities, as well as high-processing power. Compact, cost effective and with low power consumption, VAR-SOM-SOLO/DUAL secures an Intel Atom performance level.

Supporting products:

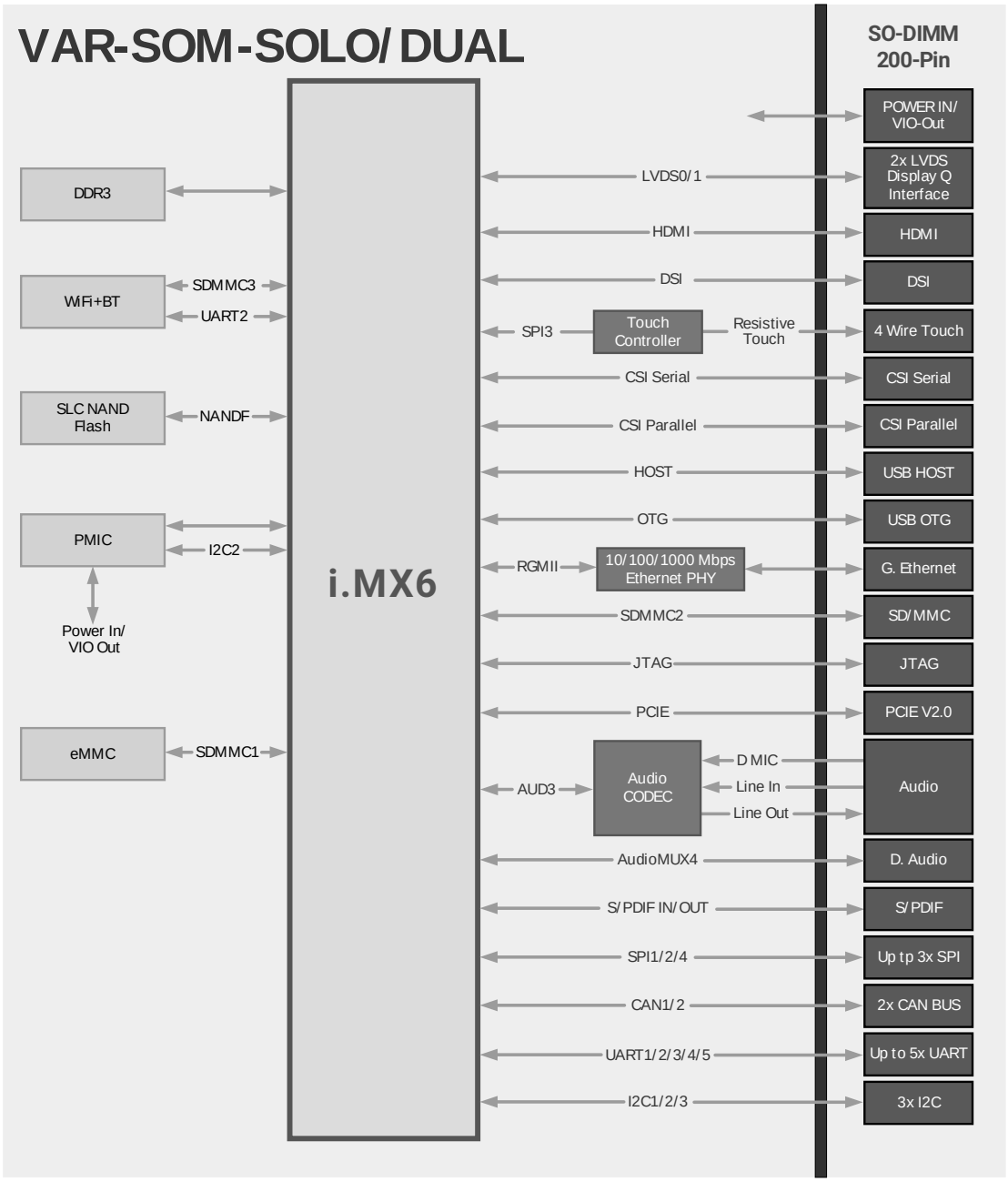
- VAR-SOLOCustomBoard – evaluation board
  - ✓ Carrier -Board, compatible with VAR-SOM-SOLO/DUAL
  - ✓ Schematics
- CSI2 Camera module
- O.S support
  - ✓ Linux BSP
  - ✓ Windows Embedded Compact 7
  - ✓ Android

Contact Variscite support services for further information: mailto:support@variscite.com.

1.2. Feature Summary

- Freescale i.MX6 series SoC Single/Dual ARM® Cortex™-A9 Core 1.0 Ghz
- Up to 1GB DDR3 RAM
- Up to 512MB NAND Flash for storage memory / boot
- Up to 128GB eMMC storage
- 2 x LVDS display interface
- HDMI V1.4 interface
- 1 x MIPI DSI
- Touch panel interface
- Parallel & serial camera interface
- On-board 10/100/1000 Mbps Ethernet PHY
- TI WiLink8 2.4/5GHz WLAN (802.11 a/b/g/n) / BT-BLE 5.1with CSA2 support and optional MIMO
- 1 x USB 2.0 host, 1 x OTG
- 1 x SD/MMC
- Serial interfaces (SPI , I2C, UART, I2S,)
- CAN Bus
- Stereo line-In / headphones out
- Digital microphone
- Single 3.3 V power supply
- 67mm x 33mm, 200 pin SO-DIMM Connector

1.3. Block Diagram



1.4. VAR-SOM-SOLO/DUAL V1.X vs VAR-SOM-MX6 V2.X

a) 40 Pin header removed
b) No SATA (i.MX6 solo/DualLite)
c) Pin-out changes on the 200 pin SODIMM connector:

Pin #	VAR-SOM-MX6 V2.X	VAR-SOM-SOLO/DUAL V1.X
30	VCC_RTC	N.C.
70	GPIO2_14 |Ball B20	JTAG_TRSTB|C2
91	SATA_RXN| Ball A14	JTAG_TDI| Ball G5
93	SATA_RXP| Ball B14	JTAG_TDO| Ball G6
97	SATA_TXP| Ball A12	JTAG_TCK| Ball H5
99	SATA_TXN| Ball B12	JTAG_TMS| Ball C3

2. Main Hardware Components

This section summarizes the main hardware building blocks of the VAR-SOM-SOLO/DUAL

2.1. Freescale i.MX6

2.1.1. Overview

The i.MX6 Solo/DualLite processor represent Freescale Semiconductor's latest achievement in integrated multimedia applications processors, optimized for lowest power consumption. The processor feature Freescale's advanced implementation of ARM™ Cortex-A9 core, which operates at speeds of up to 1 GHz. It includes 2D and 3D graphics processors, 3D 1080p video processing and integrated power management. DDR3-800bps memory interface and a number of other interfaces such as WLAN, Bluetooth™, GPS, hard drive, displays, and camera sensors.

2.1.2. CPU Platform

The i.MX6 Application Processor (AP) is based on the ARM Cortex-A9 MPCore™ Platform, which has the following features:

- ARM Cortex A9 (with TrustZone)
- Symmetric CPU configuration where each CPU includes:
  - 32 Kbyte L1 Instruction Cache
  - 32 Kbyte L1 Data Cache
  - Private Timer and Watchdog
  - Cortex-A9 NEON MPE (Media Processing Engine) Co-processor.
- The ARM Cortex A9 Core™ complex includes:
- General Interrupt Controller (GIC) with 128 interrupt support
- Global Timer
- Snoop Control Unit (SCU)
- Two Master AXI (64-bit) bus interfaces output of L2 cache
- NEON MPE coprocessor
  - SIMD Media Processing Architecture

  - NEON register file with 32x64-bit general-purpose registers
  - NEON Integer execute pipeline (ALU, Shift, MAC)
  - NEON dual, single-precision floating point execute pipeline (FADD, FMUL)
  - NEON load/store and permute pipeline External
  - Supports single and double-precision add, subtract, multiply, divide, multiply and accumulate, and square root operations as described in the ARM VFPv3 architecture.
- Provides conversions between 16-bit, 32-bit and 64-bit floating-point formats and ARM integer word formats.

2.1.3. Memory Interfaces

The memory system consists of the following components:

- Level 1 Cache—32 KB Instruction, 32 KB Data cache per core
- Level 2 Cache—Unified instruction and data (1 MByte)
- On-Chip Memory:
  - Boot ROM, including HAB (96 KB)
  - Internal multimedia / shared, fast access RAM (OCRAM, 256 KB)
  - Secure/non-secure RAM (16 KB)
- External memory interfaces:
  - 32-bit DDR3-800
  - 8-bit NAND-Flash, including support for Raw MLC/SLC, 2 KB, 4 KB, and 8 KB page size,

2.1.4. DMA engine

The SDMA is multi-channel flexible DMA engine. It helps in maximizing system performance by off-loading the various cores in dynamic data routing. It has the following features:

- Powered by a 16-bit Instruction-Set micro-RISC engine
- Multi-channel DMA supporting up to 32 time-division multiplexed DMA channels
- 48 events with total flexibility to trigger any combination of channels
- Memory accesses including linear, FIFO, and 2D addressing
- Shared peripherals between ARM and SDMA
- Very fast Context-Switching with 2-level priority based preemptive multi-tasking
- DMA units with auto-flush and prefetch capability
- Flexible address management for DMA transfers (increment, decrement, and no address changes on source and destination address)
- DMA ports can handle unit-directional and bi-directional flows (copy mode)
- Up to 8-word buffer for configurable burst transfers
- Support of byte-swapping and CRC calculations
- Library of Scripts and API is available

2.1.5. Display Subsystem

The i.MX6 Solo/DualLite video graphics subsystem consists of the following dedicated modules:

- Video Processing Unit (VPU): a multi-standard high performance video/image CODEC
- Three Graphics Processing Units (GPUs):
  - 3D GPU: accelerating the generation of 3D graphics (OpenGL/ES) and vector graphics (OpenVG)
  - 2D GPU: acceleration the generation of 2D graphics (BitBLT).
  - OpenVG: acceleration of vector graphics (OpenVG).
- Display interface bridges: providing optional translation from the digital display interface supported by the IPU to other interfaces:
  - LVDS bridge (LDB): providing up to two LVDS interfaces
  - HDMI transmitter
  - MIPI/DSI transmitter
- MIPI/CSI-2 receiver
- Two (identical) Display Content Integrity Checker (DCIC) are used to authenticate sensitive displayed data.
- A Video Data Order Adapter (VDOA): used to re-order video data from the "tiled" order used by the VPU to the conventional raster-scan order needed by the IPU.

2.1.6. MIPI - Camera Serial Interface Host Controller

The MIPI CSI-2 Host Controller supports the following features:

- Compliant with MIPI Alliance Standard for Camera Serial Interface 2 (CSI-2), Version 1.00 - 29 November 2005
- Optional support for Camera Control Interface (CCI) through the use of DesignWare Core (DW_apb_i2c)
- Interface with MIPI D-PHY following PHY Protocol Interface (PPI), as defined in MIPI Alliance Specification for D-PHY, Version 1.00.00 - 14 May 2009
- Supports up to 2 D-PHY Rx Data Lanes
- Dynamically configurable multi-lane merging
- Long and Short packet decoding
- Timing accurate signaling of Frame and Line synchronization packets; Support for several frame formats such as:
  - General Frame or Digital Interlaced Video with or without accurate sync timing
  - Data type (Packet or Frame level) and Virtual Channel interleaving
- 32-bit Image Data Interface delivering data formatted as recommended in CSI-2 Specification
- Supports all primary and secondary data formats:
  - RGB, YUV and RAW color space definitions
  - From 24-bit down to 6-bit per pixel
  - Generic or user-defined byte-based data types
  - Error detection and correction
  - PHY level
  - Packet level
  - Line level
  - Frame level

2.1.7. 2D and 3D Graphics Processing Unit (GPU)

The GPU2D module has two independent sub-modules: R2D and V2D GPUs. Both GPU were designed to display on a variety of consumer devices. Addressable screen sizes range from small displays featured on cell phones to large 1080p high definition displays.
The GPU2D cores provide powerful graphics at low power consumption, utilizing the smallest silicon footprints. Dynamic power consumption is minimized by extensive use of localized clock gating.
Hardware acceleration is brought to numerous 2D and VG applications including graphical user interfaces (GUI), menu displays, flash animation and gaming.
The GPU3D is a high-performance core that delivers hardware acceleration for 3D graphics display. Addressable screen sizes range from the smallest cell phones to HD 1080p displays. It provides high performance, high quality graphics, low power consumption and the smallest silicon footprint.
GPU3D accelerates numerous 3D graphics applications, including Graphical User Interfaces (GUI), menu displays, flash animation, and gaming. This module supports the following graphics APIs:

- OpenGL ES 2.0
- OpenGL ES 1.1

2.1.8. Audio Back End

The AUDMUX provides flexible, programmable routing of the serial interfaces (SSI1 or SSI2) to and from off-chip devices. The AUDMUX routes audio data (and even splices together multiple time-multiplexed audio streams) but does not decode or process audio data itself. The AUDMUX is controlled by the ARM but can route data even when the ARM is in a low-power mode.
The ESAI (Enhanced Serial Audio Interface) provides a full-duplex serial port for serial communication with a variety of serial devices, including industry-standard codecs, SPDIF transceivers, and other processors. The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator. The ESAI is connected to the IOMUX and to the ESAI_BIFIFO module.
The ESAI_BIFIFO (ESAI Bus Interface and FIFO) is the interface between the ESAI module and the shared peripheral bus. It contains the FIFOs used to buffer data to and from the ESAI, as well as providing the data word alignment and padding necessary to match the 24-bit data bus of the ESAI to the 32-bit data bus of the shared peripheral bus.
The SPDIF (Sony/Philips Digital Interface) audio module is a stereo transceiver that allows the processor to receive and transmit digital audio over it. The SPDIF receiver section includes a frequency measurement block that allows the precise measurement of incoming sampling frequency. A recovered clock is provided by the SPDIF receiver section and may be used to drive both internal and external components in the system. The SPDIF is connected to the shared peripheral bus.
The ASRC (Asynchronous Sample Rate Converter) converts the sampling rate of a signal associated to an input clock into a signal associated to a different output clock. The ASRC supports concurrent sample rate conversions of up to 10 channels of over 120dB THD+N. The sample rate conversion of each channel is associated to a pair of incoming and outgoing sampling rates. The ASRC supports up to three sampling rate pairs. The ASRC is connected to the shared peripheral bus.

2.1.9. 10/100/1000 Ethernet Controller

The MAC-NET core, in conjunction with a 10/100/1000 MAC, implements layer 3 network acceleration functions. These functions are designed to accelerate the processing of various common networking protocols, such as IP, TCP, UDP and ICMP, providing wire speed services to client applications. The MAC operation is fully programmable and can be used in NIC (Network Interface Card), bridging, or switching applications. The core implements the remote network monitoring (RMON) counters according to IETF RFC 2819. The core also implements a hardware acceleration block to optimize the performance of network controllers providing IP and TCP, UDP, ICMP protocol services. The acceleration block performs critical functions in hardware, which are typically implemented with large software overhead. The core implements programmable embedded FIFOs that can provide buffering on the receive path for loss-less flow control .Advanced power management features are available with magic packet detection and programmable power-down modes.

2.2. Memory

2.2.1. RAM

The VAR-SOM-SOLO/DUAL is available with up to 1GB of DDR3 memory.

2.2.2. Non-volatile Storage Memory

- NAND flash: The VAR-SOM-SOLO/DUAL is available with up to 0.5GB of SLC NAND FLASH memory. The NAND flash is used for Flash Disk purposes, O.S. run-time-image and the Boot-loader (Boot from NAND).
- eMMC : Up to 128GB of storage. Boot from eMMC is not possible, therefore minimal NAND-flash of 128MB is required.

2.3. 10/100/1000 Mbps Ethernet Transceiver

The VAR-SOM-SOLO/DUAL can be ordered with an Integrated Ethernet Transceiver, Micrel KSZ9031 or Analog Devices ADIN1300.
Please contact sales@variscite.com for inquiries about P/N assembled on your SOM.

2.3.1. Micrel KSZ9031 Ethernet Transceiver

The KSZ9031RN is a completely integrated triple speed (10Base-T/100Base-TX/1000Base-T) Ethernet Physical Layer Transceiver for transmission and reception of data over standard CAT-5 unshielded twisted pair (UTP) cable. The KSZ9031RN provides the Reduced Gigabit Media Independent Interface (RGMII) for direct connection to RGMII MACs in Gigabit Ethernet processors and switches for data transfer at 10/100/1000 Mbps speed.

2.3.2. Analog Devices ADIN1300 Ethernet Transceiver

Key features include:

- 10BASE-Te/100BASE-TX/1000BASE-T IEEE® 802.3™ compliant MII, RMII, and RGMII MAC interfaces
- EEE in accordance with IEEE 802.3az
- Start of packet detection for IEEE 1588 time stamp support
- Enhanced link detection
- Configurable LED
- Integrated power supply monitoring and POR
- MII management interface (MDIO) compatible with the IEEE 802.3 Standard Clause 22 and Clause 45 management frame structures.
- Supports cable lengths up to 150 meters at Gigabit speeds and 180 meters when operating at 100 Mbps or 10 Mbps.
- Automatic MDI/MDIX crossover
- Autonegotiation capability in accordance with IEE 802.3 Clause 28
- Supports a number of power-down modes: hardware, software, and energy detect power-down, and EEE LPI mode
- On-chip cable diagnostics capabilities
- Transmit drivers are voltage mode with on-chip terminations

2.4. TLV320AIC3106 Audio

The Texas Instrument's TLV320AIC3106 is a low-power, highly integrated stereo audio codec with stereo headphone amplifier, as well as multiple inputs and outputs programmable in single-ended or fully differential configurations. Extensive register-based power control is included, enabling stereo 48-kHz DAC playback as low as 15mW. The VAR-SOM-SOLO/DUAL exposes the following interface of the TLV320AIC3106:

- Headphone
- Line-in
- Digital microphone

2.5. Wi-Fi + BT

The VAR-SOM-SOLO/DUAL contains TI's WL183xMOD WiLink, a high performance 2.4/5 GHz IEEE 802.11 a/b/g/n Bluetooth 5.1/BLE with CSA2 support radio module, with optional Dual Band and MIMO support.
The modules support improved performance over WiFi in bit rates reaching 100Mbps (UDP) and 80Mbps (TCP).
The module realizes the necessary PHY/MAC layers to support WLAN applications in conjunction with a host processor over a SDIO interface.
The module also provides a Bluetooth platform through the HCI transport layer. Both WLAN and Bluetooth share the same antenna port.

- IEEE 802.11 b,g,n or Dual Band 2.4/5GHz 802.11 a/b/g/n with optional MIMO
- Bluetooth 5.1/BLE with CSA2 support
- U.FL connectors for external antennas
- Integrated band-pass filter
- Operating Temperature Range:
  Dual Band 2.4/5GHz Modules: -40 to +85
  2.4GHz Modules: -20 to +70

3. External Connectors

The VAR-SOM-SOLO/DUAL exposes a 200-pin SO–DIMM mechanical standard interface. The recommended mating connector for baseboard interfacing are:

1. CONCRAFT - 0701A0BE52E
2. Tyco Electronics -1565917-4

Pin#:
Pin number on the SO-DIMM200 connector

Pin Name:
Default VAR-SOM-SOLO/DUAL pin name

Type:
Pin type & direction:

- I – In
- O – Out
- DS – Differential Signal
- A – Analog
- Power – Power Pin

Pin Group:
Pin functionality group

i.MX6 Ball:
Ball number

Mode (Tables 3.2 & 3.4):
Pin mux mode option

3.1. VAR-SOM-SOLO/DUAL Connector Pin-out

Pin #	Pin Name	Type	Pin Group	GPIO	i.MX6 Ball
1	GND	POWER	Digital GND		
2	GND	POWER	Digital GND		
3	MDI_A+	DS	Gigabit Ethernet		
4	MDI_C+	DS	Gigabit Ethernet		
5	MDI_A-	DS	Gigabit Ethernet		
6	MDI_C-	DS	Gigabit Ethernet		
7	GND	POWER	Digital GND		
8	GND	POWER	Digital GND		
9	MDI_B+	DS	Gigabit Ethernet		
10	MDI_D+	DS	Gigabit Ethernet		
11	MDI_B-	DS	Gigabit Ethernet		
12	MDI_D-	DS	Gigabit Ethernet		
13	GND	POWER	Digital GND		
14	GND	POWER	Digital GND		
15	GETH_LED2	O	Gigabit Ethernet LED		
16	GETH_LED1	O	Gigabit Ethernet LED[5]	GPIO1[28]	V21
17	PWM0	IO	Pulse width modulation	GPIO4[30]	T25
18	DMIC_CLK	O	Digital microphone interface		
19	GND	POWER	Digital GND		
20	DMIC_DATA	I	Digital microphone interface		
21	AUDMUX4_RXD	IO	Digital audio mux	GPIO5[17]	W24
22	AUDMUX4_RXC	IO	Digital audio mux	GPIO5[13]	U23
23	AUDMUX4_RXFS	IO	Digital audio mux	GPIO5[12]	V25
24	AUDMUX4_TXFS	IO	Digital audio mux	GPIO5[16]	V24
25	AUDMUX4_TXC	IO	Digital audio mux	GPIO5[14]	U22
26	AUDMUX4_TXD	IO	Digital audio mux	GPIO5[15]	T20
27	GND	POWER	Digital GND		
28	GND	POWER	Digital GND		
29	CLKO2	O	Reference clock out	GPIO1[3]	R7
30	NC		Leave not connected		
31	GND	POWER	Digital GND		
32	VIN_3V3	POWER	3.3 V power supply IN		
33	GND	POWER	Digital GND		
34	VIN_3V3	POWER	3.3 V power supply IN		
35	GND	POWER	Digital GND		
36	VIN_3V3	POWER	3.3 V power supply IN		
37	GND	POWER	Digital GND		
38	VIN_3V3	POWER	3.3 V power supply IN		

Pin #	Pin Name	Type	Pin Group	GPIO	i.MX6 Ball
39	CSPI1_CS0	IO	Configurable SPI	GPIO4[9]	U6
40	BOOT_SEL1	IO	EIM_DA05	GPIO3[5]	L23
41	CSPI1_MISO	IO	Configurable SPI	GPIO4[8]	U7
42	BOOT_SEL0	IO	EIM_DA7	GPIO3[7]	L25
43	CSPI1_CLK	IO	Configurable SPI	GPIO4[6]	W5
44	CAN1_TX	IO	Controller area network	GPIO1[7]	R3
45	CSPI1_MOSI	IO	Configurable SPI	GPIO4[7]	V6
46	CAN1_RX	IO	Controller area network	GPIO1[8]	R5
47	GND	POWER	Digital GND		
48	CSPI1_CS1	IO	Configurable SPI	GPIO4[10]	W6
49	3V3_PER	POWER	Power good indication		
50*	UART2_CTS	IO	UART2 port[2]	GPIO3[28]	G23
51*	UART2_RTS	IO	UART2 port[2]	GPIO3[29]	J19
52	UART2_TXD	IO	UART2 port[2]	GPIO3[26]	E24
53	UART2_RXD	IO	UART2 port[2]	GPIO3[27]	E25
54	UART3_RXD	IO	UART3 port	GPIO3[25]	G22
55	UART3_CTS	IO	UART3 port	GPIO3[23]	D25
56	UART3_TXD	IO	UART3 port	GPIO3[24]	F22
57	UART3_RTS	IO	UART3 port[3]	GPIO2[31]	F23
58	GND	POWER	Digital GND		
59	GND	POWER	Digital GND		
60	SD2_CLK	IO	SD/MMC and SDXC	GPOP1[10]	C21
61	SD2_DATA2	IO	SD/MMC and SDXC	GPIO1[13]	A23
62	SD2_DATA0	IO	SD/MMC and SDXC	GPIO1[15]	A22
63	SD2_DATA1	IO	SD/MMC and SDXC	GPIO1[14]	E20
64	SD2_CMD	O	SD/MMC and SDXC	GPIO1[11]	F19
65	SD2_DATA3	IO	SD/MMC and SDXC	GPIO1[12]	B22
66	GND	POWER	Digital GND		
67	GND	POWER	Digital GND		
68	PWM1_OUT	IO	General purpose	GPIO1[9]	T2
69	PWM3_OUT	IO	General purpose	GPIO2[9]	B19
70	JTAG_TRSTB				
71	GPIO1_2	IO	General purpose	GPIO1[2]	T1
72	USB_OTG_ID	IO	General purpose	GPIO1[1]	T4
73	GPIO2_11	IO	General purpose	GPIO2[11]	A20
74	NC		Leave not connected		
75	SPDIFIN	IO	SPDIF	GPIO3[21]	H20
76	GND	POWER	Digital GND		
77	SPDIFOUT	IO	SPDIF	GPIO3[22]	E23

Pin #	Pin Name	Type	Pin Group	GPIO	i.MX6 Ball
78	GND	POWER	Digital GND		
79	USB_H1_OC	IO	USB host	GPIO3[30]	J20
80	CAN2_TX_OTG_OC	IO	FlexCAN-2	GPIO4[14]	T6
81	CSI0_HSYNCH	IO	Camera interface	GPIO5[19]	P4
82	CAN2_RX	IO	FlexCAN-2	GPIO4[15]	V5
83	UART1_RX	IO	UART1 port	GPIO5[29]	M3
84	UART1_RTS	IO	UART1 port	GPIO3[20]	G20
85	UART1_TX	IO	UART1 port	GPIO5[28]	M1
86	UART1_CTS	IO	UART1 port	GPIO3[19]	G21
87	I2C1_SDA	IO	I2C interface	GPIO5[26]	N6
88	I2C1_SCL	IO	I2C interface	GPIO5[27]	N5
89	GND	POWER	Digital GND		
90	I2C3_SDA	IO	I2C interface	GPIO7[11]	R2
91	JTAG_TDI				
92	I2C3_SCL	IO	I2C interface	GPIO1[5]	R4
93	JTAG_TDO				
94	GPIO1[4]	IO	USB on-the-go	GPIO1[4]	R6
95	GND	POWER	Digital GND		
96	CSI0_DAT19	IO	Camera interface	GPIO6[5]	L6
97	JTAG_TCK				
98	POR_B	I	Reset[4]		C11
99	JTAG_TMS				
100	CLK1_N	DS	PCIE clock		C7
101	GND	POWER	Digital GND		
102	CLK1_P	DS	PCIE clock		D7
103	VIN_3V3	POWER	Main power supply		G15
104	USB_H1_VBUS	I	USB 2.0 5V indication		D10
105	VIN_3V3	POWER	Main power supply		G15
106	USB_OTG_VBUS	I	OTG 5V indication		E9
107	VIN_3V3	POWER	Main power supply		G15
108	USB_HOST_DN	DS	USB host		F10
109	VIN_3V3	POWER	Main power supply		G15
110	USB_HOST_DP	DS	USB host		E10
111	VIN_3V3	POWER	Main power supply		G15
112	GND	POWER	Digital GND		
113	CSI0_DAT18	IO	Camera interface	GPIO6[4]	M6
114	USB_OTG_DN	DS	USB on-the-go		B6
115	CSI0_DAT15	IO	Camera interface	GPIO6[1]	M5
116	USB_OTG_DP	DS	USB on-the-go		A6
117	CSI0_DAT17	IO	Camera interface	GPIO6[3]	L3

Pin #	Pin Name	Type	Pin Group	GPIO	i.MX6 Ball
118	GND	POWER	Digital GND		
119	CSI_D0P	DS	Camera serial interface		E3
120	CSI0_VSYNC	IO	Camera interface	GPIO5[21]	N2
121	CSI_D0M	DS	Camera serial interface		E4
122	CSI0_DATA_EN	IO	Camera interface	GPIO5[20]	P3
123	CSI_D1M	DS	Camera serial interface		D1
124	CSI0_DAT12	IO	Camera interface	GPIO5[30]	M2
125	CSI_D1P	DS	Camera serial interface		D2
126	GND	POWER	Digital GND		
127	NC				
128	PCIE_TXM	DS	PCI express interface		A3
129	NC				
130	PCIE_TXP	DS	PCI express interface		B3
131	NC				
132	GND	POWER	Digital GND		
133	NC				
134	PCIE_RXP	DS	PCI express interface		B2
135	CSI_CLK0P	DS	Camera serial interface		F3
136	PCIE_RXM	DS	PCI express interface		B1
137	CSI_CLK0M	DS	Camera serial interface		F4
138	GND	POWER	Digital GND		
139	GND	POWER	Digital GND		
140	DSI_CLK0P	DS	Display serial interface		H4
141	DSI_D0M	DS	Display serial Interface		G2
142	DSI_CLK0M	DS	Display serial interface		H3
143	DSI_D0P	DS	Display serial interface		G1
144	GND	POWER	Digital GND		
145	DSI_D1M	DS	Display serial interface		H2
146	HDMI_D1P	DS	HDMI		J4
147	DSI_D1P	DS	Display serial interface		H1
148	HDMI_D1M	DS	HDMI		J3
149	GND	POWER	Digital GND		
150	HDMI_CLKM	DS	HDMI		J5
151	HDMI_D2P	DS	HDMI		K4
152	HDMI_CLKP	DS	HDMI		J6
153	HDMI_D2M	DS	HDMI		K3
154	HDMI_HPD	DS	HDMI		K1
155	HDMI_D0P	DS	HDMI		K6
156	HDMI_DDCCEC	IO	HDMI		K2
157	HDMI_D0M	DS	HDMI		K5

Pin #	Pin Name	Type	Pin Group	GPIO	i.MX6 Ball
158	GND	POWER	Digital GND		
159	GND	POWER	Digital GND		
160	LVDS0_TX1_N	DS	LVDS display bridge		U4
161	LVDS0_TX0_N	DS	LVDS display bridge		U2
162	LVDS0_TX1_P	DS	LVDS display bridge		U3
163	LVDS0_TX0_P	DS	LVDS display bridge		U1
164	LVDS0_TX2_N	DS	LVDS display bridge		V2
165	LVDS0_TX3_N	DS	LVDS display bridge		W2
166	LVDS0_TX2_P	DS	LVDS display bridge		V1
167	LVDS0_TX3_P	DS	LVDS display bridge		W1
168	LVDS0_CLK_N	DS	LVDS display bridge		V4
169	GND	POWER	Digital GND		
170	LVDS0_CLK_P	DS	LVDS display bridge		V3
171	CSI0_DAT14	IO	Camera interface	GPIO6[0]	M4
172	GND	POWER	Digital GND		
173	CSI0_DAT16	IO	Camera interface	GPIO6[2]	L4
174	I2C2_SCL	IO	I2C interface [1]		U5
175	CSI0_DAT13	IO	Camera interface	GPIO5[31]	L1
176	I2C2_SDA	IO	I2C interface [1]		T7
177	CSI0_PIXCLK	I	Camera interface	GPIO5[18]	P1
178	GND	POWER	Digital GND		
179	GND	POWER	Digital GND		
180	LVDS1_CLK_N	DS	LVDS display bridge		Y3
181	LVDS1_TX3_P	DS	LVDS display bridge		AA4
182	LVDS1_CLK_P	DS	LVDS display bridge		Y4
183	LVDS1_TX3_N	DS	LVDS display bridge		AA3
184	LVDS1_TX0_N	DS	LVDS display bridge		Y1
185	GND	POWER	Digital GND		
186	LVDS1_TX0_P	DS	LVDS display bridge		Y2
187	TS_X-	AI	Touch screen interface		
188	LVDS1_TX1_N	DS	LVDS display bridge		AA1
189	TS_X+	AI	Touch screen interface		
190	LVDS1_TX1_P	DS	LVDS display bridge		AA2
191	TS_Y+	AI	Touch screen interface		
192	LVDS1_TX2_N	DS	LVDS display bridge		AB1
193	TS_Y-	AI	Touch screen interface		
194	LVDS1_TX2_P	DS	LVDS display bridge		AB2
195	AGND	POWER	Audio GND		
196	AGND	POWER	Audio GND		
197	LINEIN1_LP	AI			

Pin #	Pin Name	Type	Pin Group	GPIO	i.MX6 Ball
198	HPLOUT	AO			
199	LINEIN1_RP	AI			
200	HPROUT	AO			

Notes:

[1] I2C2 Interface is used on-som. Pin mode can't be changed.

[2] UART2 interface is used for on SOM Bluetooth connectivity. Interface cannot be used if using Bluetooth. UART2 Pins marked with * are shared with WiFi/Bluetooth module. Pins can't be used and mode can't be altered if the WiFi/Bluetooth module is assembled.

[3] UART3 RTS pin is being latched at boot to determine boot sequence. Use with OE# buffer, and enable only after SOM is powered-up. Use reference schematics as example.

[4] A Delay should be added on POR_B to ensure POR_B is released after SOM voltage rails have stabilized. Use a voltage supervisor, see reference schematics.

[5] Pin is used for Ethernet PHY LED connection, can be used for other CPU alternate functions only if Ethernet PHY is not assembled.

3.2. SO-DIMM 200 Pin Mux

The table below summarizes the additional available functionality for each pin-in SO-DIMM 200 connector.

Pin	Ball	ALT0 MODE	ALT1 MODE	ALT2 MODE	ALT3 MODE	ALT4 MODE	ALT5 MODE	ALT6 MODE	ALT7 MODE	ALT8 MODE	ALT9 MODE
16	V21		enet.ENET_TX_EN	esai.ESAI_TX3_RX2			gpio1.GPIO1_IO28				i2c4.I2C4_SCL
17	T25	ipu1.IPU1_DISP0_DATA09	lcd.LCD_DATA09	pwm2.PWM2_OUT	wdog2.WDOG2_B		gpio4.GPIO4_IO30				
21	W24	ipu1.IPU1_DISP0_DATA23	lcd.LCD_DATA23	ecspi1.ECSPI1_SS0	audmux.AUD4_RXD		gpio5.GPIO5_IO17				
22	U23	ipu1.IPU1_DISP0_DATA19	lcd.LCD_DATA19	ecspi2.ECSPI2_SCLK	audmux.AUD5_RXD	audmux.AUD4_RXC	gpio5.GPIO5_IO13		eim.EIM_CS3		
23	V25	ipu1.IPU1_DISP0_DATA18	lcd.LCD_DATA18	ecspi2.ECSPI2_SS0	audmux.AUD5_TXFS	audmux.AUD4_RXFS	gpio5.GPIO5_IO12		eim.EIM_CS2		
24	V24	ipu1.IPU1_DISP0_DATA22	lcd.LCD_DATA22	ecspi1.ECSPI1_MISO	audmux.AUD4_TXFS		gpio5.GPIO5_IO16				
25	U22	ipu1.IPU1_DISP0_DATA20	lcd.LCD_DATA20	ecspi1.ECSPI1_SCLK	audmux.AUD4_TXC		gpio5.GPIO5_IO14				
26	T20	ipu1.IPU1_DISP0_DATA21	lcd.LCD_DATA21	ecspi1.ECSPI1_MOSI	audmux.AUD4_TXD		gpio5.GPIO5_IO15				
29	R7	esai.ESAI_RX_HF_CLK		i2c3.I2C3_SCL	xtalosc. XTALOSC_REF_CLK_24M	ccm.CCM_CLKO2	gpio1.GPIO1_IO03	usb.USB_H1_OC	mlb.MLB_CLK		
39	U6	ecspi1.ECSPI1_SS0	enet.ENET_COL	audmux.AUD5_RXD	kpp.KEY_ROW1	uart5.UART5_RX_DATA	gpio4.GPIO4_IO09	usdhc2.SD2_VSELECT			
40	L23	eim.EIM_AD05	ipu1.IPU1_DISP1_DATA04	ipu1.IPU1_CSI1_DATA04			gpio3.GPIO3_IO05		src.SRC_BOOT_CFG05	epdc.EPDC_SDCE1	
41	U7	ecspi1.ECSPI1_MISO	enet.ENET_MDIO	audmux.AUD5_TXFS	kpp.KEY_COL1	uart5.UART5_TX_DATA	gpio4.GPIO4_IO08	usdhc1.SD1_VSELECT			
42	L25	eim.EIM_AD07	ipu1.IPU1_DISP1_DATA02	ipu1.IPU1_CSI1_DATA02			gpio3.GPIO3_IO07		src.SRC_BOOT_CFG07	epdc.EPDC_SDCE3	
43	W5	ecspi1.ECSPI1_SCLK	enet.ENET_RX_DATA3	audmux.AUD5_TXC	kpp.KEY_COL0	uart4.UART4_TX_DATA	gpio4.GPIO4_IO06	dcic1.DCIC1_OUT			
44	R3	esai.ESAI_TX4_RX1		epit1.EPIT1_OUT	flexcan1.FLEXCAN1_TX	uart2.UART2_TX_DATA	gpio1.GPIO1_IO07	spdif.SPDIF_LOCK	usb. USB_OTG_HOST_MODE	i2c4.I2C4_SCL	
45	V6	ecspi1.ECSPI1_MOSI	enet.ENET_TX_DATA3	audmux.AUD5_TXD	kpp.KEY_ROW0	uart4.UART4_RX_DATA	gpio4.GPIO4_IO07	dcic2.DCIC2_OUT			
46	R5	esai.ESAI_TX5_RX0	xtalosc. XTALOSC_REF_CLK_32K	epit2.EPIT2_OUT	flexcan1.FLEXCAN1_RX	uart2.UART2_RX_DATA	gpio1.GPIO1_IO08	spdif.SPDIF_SR_CLK	usb. USB_OTG_PWR_CTL_WAKE	i2c4.I2C4_SDA	
48	W6	ecspi1.ECSPI1_SS1	enet.ENET_RX_DATA2	flexcan1.FLEXCAN1_TX	kpp.KEY_COL2	enet.ENET_MDC	gpio4.GPIO4_IO10	usb. USB_H1_PWR_CTL_WAKE			
50	G23	eim.EIM_DATA28	i2c1.I2C1_SDA	ecspi4.ECSPI4_MOSI	ipu1.IPU1_CSI1_DATA12	uart2.UART2_CTS_B	gpio3.GPIO3_IO28	ipu1.IPU1_EXT_TRIG	ipu1.IPU1_DI0_PIN13	epdc.EPDC_SDOED	
51	J19	eim.EIM_DATA29	ipu1.IPU1_DI1_PIN15	ecspi4.ECSPI4_SS0		uart2.UART2_RTS_B	gpio3.GPIO3_IO29	ipu1.IPU1_CSI1_VSYNC	ipu1.IPU1_DI0_PIN14	epdc.EPDC_SDOE	
52	E24	eim.EIM_DATA26	ipu1.IPU1_DI1_PIN11	ipu1.IPU1_CSI0_DATA01	ipu1.IPU1_CSI1_DATA14	uart2.UART2_TX_DATA	gpio3.GPIO3_IO26	ipu1.IPU1_SISG2	ipu1.IPU1_DISP1_DATA22	epdc.EPDC_SDCE8	
53	E25	eim.EIM_DATA27	ipu1.IPU1_DI1_PIN13	ipu1.IPU1_CSI0_DATA00	ipu1.IPU1_CSI1_DATA13	uart2.UART2_RX_DATA	gpio3.GPIO3_IO27	ipu1.IPU1_SISG3	ipu1.IPU1_DISP1_DATA23	epdc.EPDC_DATA11	
54	G22	eim.EIM_DATA25	ecspi4.ECSPI4_SS3	uart3.UART3_RX_DATA	ecspi1.ECSPI1_SS3	ecspi2.ECSPI2_SS3	gpio3.GPIO3_IO25	audmux.AUD5_RXC	uart1.UART1_DSR_B	epdc.EPDC_SDCE7	
55	D25	eim.EIM_DATA23	ipu1.IPU1_DI0_D0_CS	uart3.UART3_CTS_B	uart1.UART1_DCD_B	ipu1.IPU1_CSI1_DATA_EN	gpio3.GPIO3_IO23	ipu1.IPU1_DI1_PIN02	ipu1.IPU1_DI1_PIN14	epdc.EPDC_SDCE0	eim.EIM_ACLK_FREERUN
56	F22	eim.EIM_DATA24	ecspi4.ECSPI4_SS2	uart3.UART3_TX_DATA	ecspi1.ECSPI1_SS2	ecspi2.ECSPI2_SS2	gpio3.GPIO3_IO24	audmux.AUD5_RXFS	uart1.UART1_DTR_B		

Pin	Ball	ALT0 MODE	ALT1 MODE	ALT2 MODE	ALT3 MODE	ALT4 MODE	ALT5 MODE	ALT6 MODE	ALT7 MODE	ALT8 MODE	ALT9 MODE
57	F23	eim.EIM_EB3	ecspi4.ECSPI4_RDY	uart3.UART3_RTS_B	uart1.UART1_RI_B	ipu1.IPU1_CSI1_HSYNC	gpio2.GPIO2_IO31	ipu1.IPU1_DI1_PIN03	src.SRC_BOOT_CFG31		
60	C21	usdhc2.SD2_CLK		kpp.KEY_COL5	audmux.AUD4_RXFS		gpio1.GPIO1_IO10				
61	A23	usdhc2.SD2_DATA2		eim.EIM_CS3	audmux.AUD4_TXD	kpp.KEY_ROW6	gpio1.GPIO1_IO13				
62	A22	usdhc2.SD2_DATA0			audmux.AUD4_RXD	kpp.KEY_ROW7	gpio1.GPIO1_IO15	dcic2.DCIC2_OUT			
63	E20	usdhc2.SD2_DATA1		eim.EIM_CS2	audmux.AUD4_TXFS	kpp.KEY_COL7	gpio1.GPIO1_IO14				
64	F19	usdhc2.SD2_CMD		kpp.KEY_ROW5	audmux.AUD4_RXC		gpio1.GPIO1_IO11				
65	B22	usdhc2.SD2_DATA3		kpp.KEY_COL6	audmux.AUD4_TXC		gpio1.GPIO1_IO12				
68	T2	esai.ESAI_RX_FS	wdog1.WDOG1_B	kpp.KEY_COL6	ccm.CCM_REF_EN_B	pwm1.PWM1_OUT	gpio1.GPIO1_IO09	usdhc1.SD1_WP			
69	B19		usdhc4.SD4_DATA1	pwm3.PWM3_OUT			gpio2.GPIO2_IO09				
71	T1	esai.ESAI_TX_FS		kpp.KEY_ROW6			gpio1.GPIO1_IO02	usdhc2.SD2_WP	mlb.MLB_DATA		
72	T4	esai.ESAI_RX_CLK	wdog2.WDOG2_B	kpp.KEY_ROW5	usb.USB_OTG_ID	pwm2.PWM2_OUT	gpio1.GPIO1_IO01	usdhc1.SD1_CD_B			
73	A20		usdhc4.SD4_DATA3				gpio2.GPIO2_IO11			epdc.EPDC_SDCE6	
75	H20	eim.EIM_DATA21	ecspi4.ECSPI4_SCLK	ipu1.IPU1_DI0_PIN17	ipu1.IPU1_CSI1_DATA11	usb.USB_OTG_OC	gpio3.GPIO3_IO21	i2c1.I2C1_SCL	spdif.SPDIF_IN	epdc.EPDC_SDOEZ	
77	E23	eim.EIM_DATA22	ecspi4.ECSPI4_MISO	ipu1.IPU1_DI0_PIN01	ipu1.IPU1_CSI1_DATA10	usb.USB_OTG_PWR	gpio3.GPIO3_IO22	spdif.SPDIF_OUT			
79	J20	eim.EIM_DATA30	ipu1.IPU1_DISP1_DATA21	ipu1.IPU1_DI0_PIN11	ipu1.IPU1_CSI0_DATA03	uart3.UART3_CTS_B	gpio3.GPIO3_IO30	usb.USB_H1_OC			
80	T6	flexcan2.FLEXCAN2_TX	ipu1.IPU1_SISG4	usb.USB_OTG_OC	kpp.KEY_COL4	uart5.UART5_RTS_B	gpio4.GPIO4_IO14				
81	P4	ipu1.IPU1_CSI0_HSYNC			ccm.CCM_CLKO1		gpio5.GPIO5_IO19		arm.ARM_TRACE_CTL		
82	V5	flexcan2.FLEXCAN2_RX	ipu1.IPU1_SISG5	usb.USB_OTG_PWR	kpp.KEY_ROW4	uart5.UART5_CTS_B	gpio4.GPIO4_IO15				
83	M3	ipu1.IPU1_CSI0_DATA11	audmux.AUD3_RXFS	ecspi2.ECSPI2_SS0	uart1.UART1_RX_DATA		gpio5.GPIO5_IO29		arm.ARM_TRACE08		
84	G20	eim.EIM_DATA20	ecspi4.ECSPI4_SS0	ipu1.IPU1_DI0_PIN16	ipu1.IPU1_CSI1_DATA15	uart1.UART1_RTS_B	gpio3.GPIO3_IO20	epit2.EPIT2_OUT		epdc.EPDC_DATA12	
85	M1	ipu1.IPU1_CSI0_DATA10	audmux.AUD3_RXC	ecspi2.ECSPI2_MISO	uart1.UART1_TX_DATA		gpio5.GPIO5_IO28		arm.ARM_TRACE07		
86	G21	eim.EIM_DATA19	ecspi1.ECSPI1_SS1	ipu1.IPU1_DI0_PIN08	ipu1.IPU1_CSI1_DATA16	uart1.UART1_CTS_B	gpio3.GPIO3_IO19	epit1.EPIT1_OUT			
87	N6	ipu1.IPU1_CSI0_DATA08	eim.EIM_DATA06	ecspi2.ECSPI2_SCLK	kpp.KEY_COL7	i2c1.I2C1_SDA	gpio5.GPIO5_IO26		arm.ARM_TRACE05		
88	N5	ipu1.IPU1_CSI0_DATA09	eim.EIM_DATA07	ecspi2.ECSPI2_MOSI	kpp.KEY_ROW7	i2c1.I2C1_SCL	gpio5.GPIO5_IO27		arm.ARM_TRACE06		
90	R2	esai.ESAI_TX3_RX2	enet.ENET_1588_EVENT2_IN	enet.ENET_REF_CLK	usdhc1.SD1_LCTL	spdif.SPDIF_IN	gpio7.GPIO7_IO11	i2c3.I2C3_SDA	sjc.JTAG_DE_B		
92	R4	esai.ESAI_TX2_RX3		kpp.KEY_ROW7	ccm.CCM_CLKO1		gpio1.GPIO1_IO05	i2c3.I2C3_SCL	arm.ARM_EVENTI		
94	R6	esai.ESAI_TX_HF_CLK		kpp.KEY_COL7			gpio1.GPIO1_IO04	usdhc2.SD2_CD_B			

Pin	Ball	ALT0 MODE	ALT1 MODE	ALT2 MODE	ALT3 MODE	ALT4 MODE	ALT5 MODE	ALT6 MODE	ALT7 MODE	ALT8 MODE	ALT9 MODE
96	L6	ipu1.IPU1_CSI0_DATA19	eim.EIM_DATA15		uart5.UART5_CTS_B		gpio6.GPIO6_IO05				
113	M6	ipu1.IPU1_CSI0_DATA18	eim.EIM_DATA14		uart5.UART5_RTS_B		gpio6.GPIO6_IO04		arm.ARM_TRACE15		
115	M5	ipu1.IPU1_CSI0_DATA15	eim.EIM_DATA11		uart5.UART5_RX_DATA		gpio6.GPIO6_IO01		arm.ARM_TRACE12		
117	L3	ipu1.IPU1_CSI0_DATA17	eim.EIM_DATA13		uart4.UART4_CTS_B		gpio6.GPIO6_IO03		arm.ARM_TRACE14		
120	N2	ipu1.IPU1_CSI0_VSYNC	eim.EIM_DATA01				gpio5.GPIO5_IO21		arm.ARM_TRACE00		
122	P3	ipu1.IPU1_CSI0_DATA_EN	eim.EIM_DATA00				gpio5.GPIO5_IO20		arm.ARM_TRACE_CLK		
124	M2	ipu1.IPU1_CSI0_DATA12	eim.EIM_DATA08		uart4.UART4_TX_DATA		gpio5.GPIO5_IO30		arm.ARM_TRACE09		
171	M4	ipu1.IPU1_CSI0_DATA14	eim.EIM_DATA10		uart5.UART5_TX_DATA		gpio6.GPIO6_IO00		arm.ARM_TRACE11		
173	L4	ipu1.IPU1_CSI0_DATA16	eim.EIM_DATA12		uart4.UART4_RTS_B		gpio6.GPIO6_IO02		arm.ARM_TRACE13		
175	L1	ipu1.IPU1_CSI0_DATA13	eim.EIM_DATA09		uart4.UART4_RX_DATA		gpio5.GPIO5_IO31		arm.ARM_TRACE10		
177	P1	ipu1.IPU1_CSI0_PIXCLK					gpio5.GPIO5_IO18		arm.ARM_EVENTO	epdc.EPDC_PWR_WAKE	

4. SOM's interfaces

4.1. Display Interfaces

4.1.2 Overview

The VAR-SOM-SOLO/DUAL consists of the following display interfaces:

- Two LVDS channels, driven by the LDB; pixel clock up to 170 MHz
- One HDMI port (ver. 1.4) - driven by the HDMI transmitter: Pixel clock up to 266 MHz (gated by the IPU capabilities)
- One MIPI/DSI port - driven by the MIPI/DSI transmitter; two data lanes @ 1 GHz
- Each IPU has two display ports. Up to four external ports can be active at any given time (additional asynchronous data flows can be sent though the parallel ports and the MIPI/DSI port).

4.1.3 DSI

VAR-SOM-SOLO/DUAL MIPI DSI Host Controller supports up to 2 D-PHY data lanes:

- Bidirectional communication and escape mode support through the data lane
- Programmable display resolutions, from 160 x 120(QQVGA) to 1024 x 768(XVGA)
- Multiple peripheral support capability, configurable virtual channels
- Video mode pixel formats, 16 bpp (5,6,5 RGB), 18 bpp (6,6,6,RGB) packed, 18 bpp (6,6,6,RGB) loosely, 24 bpp (8,8,8,RGB)

DSI signals:

Signal	Pin #	Type	Description
DSI_CLK0M	142	ODS	Negative DSI clock differential
DSI_CLK0P	140	ODS	Positive DSI clock differential
DSI_D0M	141	ODS	Negative DSI data 0 differential
DSI_D0P	143	ODS	Positive DSI data 0 differential
DSI_D1M	145	ODS	Negative DSI data 1 differential
DSI_D1P	147	ODS	Positive DSI data 1 differential

4.1.4 HDMI

The HDMI module provides an HDMI standard interface port to an HDMI 1.4 compliant display

HDMI Signals:

Signal	Pin #	Type	Description
HDMI_CLKM	150	ODS	Negative HDMI clock differential
HDMI_CLKP	152	ODS	Positive HDMI clock differential
HDMI_D0M	157	ODS	Negative HDMI data 0 differential
HDMI_D0P	155	ODS	Positive HDMI data 0 differential
HDMI_D1M	148	ODS	Negative HDMI data 1 differential
HDMI_D1P	146	ODS	Positive HDMI data 1 differential
HDMI_D2M	153	ODS	Negative HDMI data 2 differential
HDMI_D2P	151	ODS	Positive HDMI data 2 differential
HDMI_DDCCEC	156	IO	One wire bidirectional CEC
HDMI_HPD	154	I	Hot plug detect

4.1.5 LVDS Interface

LVDS Display Bridge (LDB) will be used to connect the IPU (Image Processing Unit) to the External LVDS display interface.
There are 2 LVDS channels. These outputs are used to communicate RGB data and controls to external LCD displays.
The LVDS ports may be used as follows:

- Single channel output
- Dual channel output (one input source, two channel outputs for two displays)
- Split channel output (one input source, split to two channels on output)
- Separate two channel output (two input sources from IPU)

LVDS0 Signals:

Signal	Pin #	Type	Description
LVDS0_TX0_N	161	ODS	Negative data 0 differential
LVDS0_TX0_P	163	ODS	Positive data 0 differential
LVDS0_TX1_N	160	ODS	Negative data 1 differential
LVDS0_TX1_P	162	ODS	Positive data 1 differential
LVDS0_TX2_N	164	ODS	Negative data 2 differential
LVDS0_TX2_P	166	ODS	Positive data 2 differential
LVDS0_TX3_N	165	ODS	Negative data 3 differential
LVDS0_TX3_P	167	ODS	Positive data 3 differential
LVDS0_CLK_N	168	ODS	Negative clock differential
LVDS0_CLK_P	170	ODS	Positive clock differential

Table 4-1 LVDS Signals

LVDS1 Signals:

Signal	Pin #	Type	Description
LVDS1_TX0_N	184	ODS	Negative data 0 differential
LVDS1_TX0_P	186	ODS	Positive data 0 differential
LVDS1_TX1_N	188	ODS	Negative data 1 differential
LVDS1_TX1_P	190	ODS	Positive data 1 differential
LVDS1_TX2_N	192	ODS	Negative data 2 differential
LVDS1_TX2_P	194	ODS	Positive data 2 differential
LVDS1_TX3_N	183	ODS	Negative data 3 differential
LVDS1_TX3_P	181	ODS	Positive data 3 differential
LVDS1_CLK_N	180	ODS	Negative clock differential
LVDS1_CLK_P	182	ODS	Positive clock differential

4.2. Touch Panel

The VAR-SOM-SOLO/DUAL features a 4-wire resistive touch panel interface:

- Compatible with 4-wire resistive touch screens
- Pen-detection and nIRQ generation
- Supports several schemes of measurement, averaging to filter noise

Touch-screen Controller Signals:

Signal	Pin #	Type	Description
TS_X-	187	AI	Touch screen X minus
TS_Y-	193	AI	Touch screen Y minus
TS_X+	189	AI	Touch screen X plus
TS_Y+	191	AI	Touch screen Y plus

4.3. Camera Interfaces

4.3.1. MIPI CSI-2

The CSI-2 Host Controller is a digital core that implements all protocol functions defined in the MIPI CSI-2 specification, providing an interface between the system and the MIPI D-PHY, allowing communication with an MIPI CSI-2 compliant camera sensor.

The MIPI CSI-2 host controller supports the following features:

- Compliance with MIPI Alliance standard for camera serial interface 2 (CSI-2), version 1.00 29th November, 2005
- Optional support for Camera Control Interface (CCI) through the use of DesignWare Core (DW_apb_i2c)
- Interface with MIPI D-PHY following PHY Protocol Interface (PPI), as defined in MIPI Alliance Specification for D-PHY, version 1.00.00 14th May, 2009
- Supports up to 2 D-PHY Rx data lanes
- Dynamically configurable multi-lane merging
- Long and short packet decoding
- Timing accurate signaling of frame and line synchronization packets

- Support for several frame formats such as:
  - General frame or digital interlaced video with or without accurate sync timing
  - Data type (packet or frame level) and virtual channel interleaving
- 32-bit image data interface delivering data formatted as recommended in CSI-2 specification
- Supports all primary and secondary data formats:
  - RGB, YUV and RAW color space definitions
  - From 24-bit down to 6-bit per pixel
  - Generic or user-defined byte-based data types
  - Error detection and correction:
    - PHY level
    - Packet level
    - Line level
    - Frame level

MIPI CSI-2 signals:

Signal	Pin #	Type	Description
CSI_CLK0M	137	IDS	Negative CSI-2 clock differential
CSI_CLK0P	135	IDS	Positive CSI-2 clock differential
CSI_D0M	121	IDS	Negative CSI-2 data 0 differential
CSI_D0P	119	IDS	Positive CSI-2 data 0 differential
CSI_D1M	123	IDS	Negative CSI-2 data 1 differential
CSI_D1P	125	IDS	Positive CSI-2 data 1 differential

4.3.2. Parallel CSIx

Based on i.MX6 IPU, the VAR-SOM-SOLO/DUAL supports a camera port controlled by a CSI sub-block, providing a connection to image sensors and related devices.

CSI0 can implement 12bit CSI interface.

CSI0 Signals on 200 pin SO-DIMM connector:

Signal	Pin #	Type	Description
CSI0_DAT8	87	IO	Camera data line
CSI0_DAT9	88	IO	Camera data line
CSI0_DAT10	85	IO	Camera data line
CSI0_DAT11	83	IO	Camera data line
CSI0_DAT12	124	IO	Camera data line
CSI0_DAT13	175	IO	Camera data line
CSI0_DAT14	171	IO	Camera data line
CSI0_DAT15	115	IO	Camera data line
CSI0_DAT16	173	IO	Camera data line
CSI0_DAT17	117	IO	Camera data line
CSI0_DAT18	113	IO	Camera data line
CSI0_DAT19	96	IO	Camera data line
CSI0_DATA_EN	122	IO	Camera data enable
CSI0_HSYNCH	81	IO	Camera horizontal sync
CSI0_PIXCLK	177	IO	Camera pixel clock
CSI0_VSYNC	120	IO	Camera vertical sync

4.4. Gigabit Ethernet

Gigabit Ethernet Features:

The Ethernet Media Access Controller (MAC) is designed to support 10/100/1000 Mbps Ethernet/IEEE 802.3 networks. An external Gigabit magnetics is required to complete the interface to the media. The i.MX6 processor also consists of HW assist for IEEE1588 standard. See the IEEE1588 section for more details.

Gigabit Ethernet Magnetics:

In order to utilize the VAR-SOM-SOLO/DUAL Gigabit Ethernet interface, compatible magnetics should be used on the carrier board.

Vendor	Part Number	Package	Cores	Configuration
Pulse	H5007NL	Transformer	8	Auto-MDX
TDK	TLA-7T101LF	Transformer	8	Auto-MDX
Pulse	J0G-0009NL	Integrated RJ45	8	Auto-MDX

Gigabit Ethernet Signals:

Signal	Pin #	Type	Description
MDI_A+	3	DS	Positive A differential lane
MDI_A-	5	DS	Negative A differential lane
MDI_B+	9	DS	Positive B differential lane
MDI_B-	11	DS	Negative B differential lane
MDI_C+	4	DS	Positive C differential lane
MDI_C-	6	DS	Negative C differential lane
MDI_D+	10	DS	Positive D differential lane
MDI_D-	12	DS	Negative D differential lane

4.5. Wi-Fi & Bluetooth

The VAR-SOM-SOLO/DUAL contains TI's WL183xMOD WiLink, a high performance 2.4/5 GHz IEEE 802.11 a/b/g/n Bluetooth 5.1/BLE with CSA2 support radio module, with optional Dual Band and MIMO support.
The modules support improved performance over WiFi in bit rates reaching 100Mbps (UDP) and 80Mbps (TCP).
The module realizes the necessary PHY/MAC layers to support WLAN applications in conjunction with a host processor over a SDIO interface.
The module also provides a Bluetooth platform through the HCI transport layer. Both WLAN and Bluetooth share the same antenna port.

- IEEE 802.11 b,g,n or Dual Band 2.4/5GHz 802.11 a/b/g/n with optional MIMO
- Bluetooth 5.1/BLE with CSA2 support
- U.FL connectors for external antennas
- Integrated band-pass filter
- Operating Temperature Range:
  Dual Band 2.4/5GHz Modules: -40 to +85
  2.4GHz Modules: -20 to +70

WL1831 – Populate ANT1 only

4.6. USB Host 2.0

The USB controller block provides high performance USB functionality that conforms to the USB 2.0 specification.

USB Host1 Signals:

Signal	Pin #	Type	Description
USB_HOST_DP	110	IODS	Positive USB host data
USB_HOST_DN	108	IODS	Negative USB host data
USB_H1_VBUS	104	I	USB 2.0 VBUS indicator (5V)
USB_H1_OC	79	I	USB host over current indicator , Active low 3.3v digital

4.7. USB 2.0 OTG

USB 2.0 On-the-go Features:

High-speed OTG core

- HS/FS/LS UTMI compliant interface
- High speed, full speed and low speed operation in host mode (with UTMI transceiver)
- High speed, and full speed operation in peripheral mode (with UTMI transceiver)
- Hardware support for OTG signaling, session request protocol, and host negotiation protocol
- Up to 8 bidirectional endpoints
- Integrated HS USB PHY

OTG Signals:

Signal	Pin #	Type	Description
USB_OTG_DN	114	IODS	Negative USB OTG data
USB_OTG_DP	116	IODS	Positive USB OTG data
USB_OTG_VBUS	106	I	USB 2.0 OTG VBUS indicator (5V)
USB_OTG_ID	72	I	USB OTG host/client ID Low : Host mode Float: Client mode

4.8. MMC/SD/SDIO

MX6 MMC interface features:

- Fully compliant with MMC command/response sets and physical layer as defined in the Multimedia Card System specification v4.2/4.3/4.4/.41, including high-capacity (size > 2 GB) cards HC MMC.
- Fully compliant with SD command/response sets and physical layer as defined in the SD Memory Card specifications v2.0, including high-capacity SDHC and extended-capacity SDXC cards.
- Fully compliant with SDIO command/response sets and interrupt/read-wait mode as defined in the SDIO Card specification, Part E1 v1.10

- Fully compliant with SD Card specification, Part A2, SD Host Controller Standard specification v2.00
- 1-bit or 4-bit transfer mode specifications for MMC/SD/SDIO cards up to HS mode (25MB/s max)

SDMMC2 Signals:

Signal	Pin #	Type	Description
SD2_CLK	60	O	Clock for MMC/SD/SDIO card
SD2_CMD	64	IO	CMD line connect to card
SD2_DATA0	62	IO	DAT0 line in all modes (also used to detect busy state)
SD2_DATA1	63	IO	DAT1 line-in
SD2_DATA2	61	IO	DAT2 line
SD2_DATA3	65	IO	DAT3 line-in

4.9. Audio

The VAR-SOM-SOLO/DUAL features three audio interfaces:

- TLV320AIC3106 Audio codec interfaces
    1. Analog outputs / inputs:
        - stereo line-in
        - Stereo HP out
    2. Digital microphone input
- SSI Digital audio interface
- S/PDIF in/out

Analog audio signals are featured by the on-SOM TLV320AIC3106 audio codec. Refer to the data sheet for detailed electrical characteristics of the relevant interfaces http://www.ti.com/product/tlv320aic3106.

Analog Signals:

Signal	Pin #	Type	Description
HP_LOUT	198	AO	Headphones out - left
HP_ROUT	200	AO	Headphones out - right
LINEIN1_LP	197	AI	Line-in - Right
LINEIN1_RP	199	AI	Line-in - Left

Digital AUDMUX:

Key features of the block include:

- Full 6-wire SSI interfaces for asynchronous receive and transmit
- Configurable 4-wire (synchronous) or 6-wire (asynchronous) peripheral interfaces
- Independent Tx/Rx frame sync and clock direction selection for host or peripheral
- Each host interface's capability to connect to any other host or peripheral interface in a point-to-point or point-to-multipoint (network mode)
- Transmit and receive data switching to support external network mode

AUDMUX4 Signals:

Signal	Pin #	Type	Description
AUDMUX4_TXD	26	IO	Transmit data from pin
AUDMUX4_RXD	21	IO	Receive data at pin
AUDMUX4_TXC	25	IO	Transmit clock input/output at pin
AUDMUX4_RXC	22	IO	Receive clock input/output at pin
AUDMUX4_TXFS	24	IO	Transmit frame sync input/output at pin
AUDMUX4_RXFS	23	IO	Receive frame sync input/output at pin

S/PDIF (Sony Phillips Digital Interface) In/Out:

S/PDIF is a standard audio file transfer format, developed jointly by the Sony and Phillips corporations.

SPIDF Signals:

Signal	Pin #	Type	Description
SPDIFIN	75		In
SPDIFOUT	77		Out
Spdif.plock	44(MUXED)		
Spdif.srclk	46(MUXED)		Clock

4.10. UART Interfaces

All 5 UART interfaces are supported, refer to Table 3.2 for pin mux configurations of the UART interface.

UART Features:

- High-speed TIA/EIA-232-F compatible, up to 5.0 Mbit/s
- Serial IR interface low-speed, IrDA-compatible (up to 115.2 Kbit/s)
- 9-bit or Multidrop mode (RS-485) support (automatic slave address detection)
- 7 or 8 data bits for RS-232 characters, or 9 bit RS-485 format
- 1 or 2 stop bits
- Programmable parity (even, odd, and no parity)
- Hardware flow control support for request to send (RTS_B) and clear to send (CTS_B) signals
- RS-485 driver direction control via CTS_B signal
- Auto baud rate detection (up to 115.2 Kbit/s)
- DCE/DTE capability
- Two independent, 32-entry FIFOs for transmit and receive

UART1 Signals:

Signal	Pin #	Type	Description
UART1_CTS	86	O	UART HW flow control RTS
UART1_RTS	84	I	UART HW flow control CTS
UART1_TX	85	O	UART transmit
UART1_RX	83	I	UART receive

Note: UART1 is used as default boot debug port.

UART2 Signals:

Signal	Pin #	Type	Description
UART2_TXD	44 52	O	UART transmit
UART2_RXD	46 53	I	UART receive
UART2_RTS	51*	I	UART HW flow control RTS
UART2_CTS	50*	O	UART HW flow control CTS

Note:
UART2 is used for by on SOM Bluetooth. Interface cannot be used if using Bluetooth.
Pins marked with * are shared with WiFi/Bluetooth module. Pins can't be used and mode can't be altered if the WiFi/Bluetooth module is assembled.

UART3 Signals:

Signal	Pin #	Type	Description
UART3_TXD	56	O	UART transmit
UART3_RXD	54	I	UART receive
UART3_RTS[1]	57	I	UART HW flow control RTS
UART3_CTS	55 79	O	UART HW flow control CTS

[1] UART3 RTS pin is being latched at boot to determine boot sequence. Use with OE# buffer, and enable only after SOM is powered-up. Use reference schematics as example.

UART4 Signals:

Signal	Pin #	Type	Description
UART4_TXD	43 124	O	UART transmit
UART4_RXD	45 175	I	UART receive
UART4_RTS	173	I	UART HW flow control RTS
UART4_CTS	117	O	UART HW flow control CTS

UART5 Signals:

Signal	Pin #	Type	Description
UART5_TXD	41 171	O	UART transmit
UART5_RXD	39 115	I	UART receive
UART5_RTS	80 113	I	UART HW flow control RTS
UART5_CTS	82 96	O	UART HW flow control CTS

4.11. Flexible Controller Area Network (FLEXCAN)

The CAN protocol was primarily, but not exclusively, designed to be used as a vehicle serial data bus, meeting the specific requirements of this field: Real-time processing, reliable operation in the Electromagnetic Interference (EMI) environment of a vehicle, cost-effectiveness and required bandwidth. The FlexCAN module is a full implementation of the CAN protocol specification, version 2.0 B, which supports both standard and extended message frames.

CAN1 Signals:

Signal	Pin #	Type	Description
CAN1_RX	46	I	CAN BUS receive
CAN1_TX	44	O	CAN BUS transmit

CAN2 Signals:

Signal	Pin #	Type	Description
CAN2_TX	80	O	CAN BUS receive
CAN2_RX	82	I	CAN BUS transmit

Signal Descriptions
CAN Rx: The receive pin from the CAN bus transceiver. Dominant state is represented by logic level '0'. Recessive state is represented by logic level '1'.
CAN Tx: The transmit pin to the CAN bus transceiver. Dominant state is represented by logic level '0'. Recessive state is represented by logic level '1'.

4.12. SPI

The Enhanced Configurable Serial Peripheral Interface (ECSPI) is a full-duplex, synchronous 4-wire serial communication block. The ECSPI contains a 64 x 32 receive buffer (RXFIFO) and a 64 x 32 transmit buffer (TXFIFO). With data FIFOs, the ECSPI allows rapid data communication with fewer software interruptions.

4.12.1. eCSPI Key Features:

- Full-duplex synchronous serial interface
- Master/slave configurable
- Four chip select (SS) signals to support multiple peripherals
- Transfer continuation function allows unlimited length data transfers
- 32-bit wide by 64-entry FIFO for both transmitting and receiving data
- 32-bit wide by 16-entry FIFO for HT message data
- Polarity and phase of the chip select (SS) and SPI clock (SCLK) are configurable
- Direct Memory Access (DMA) support
- Max operation frequency up to the reference clock frequency

ECSPI1 Signals:

Signal	Pin #	Type	Description
cSPI1_CLK	25, 43	IO	SPI1 clock
cSPI1_MOSI	26, 45	IO	SPI1 MOSI signal
cSPI1_MISO	24, 41	IO	SPI1 SOMI signal
cSPI1_CS0	39, 21	IO	SPI1 chip select 0 signal
cSPI1_CS1	48, 86	IO	SPI1 chip select 1 signal
cSPI1_CS2	56	IO	SPI1 chip select 2 signal
cSPI1_CS3	54, 174	IO	SPI1 chip select 3 signal

ECSPI2 Signals:

Signal	Pin #	Type	Description
cSPI2_CLK	22, 87	IO	SPI2 clock
cSPI2_MOSI	88	IO	SPI2 MOSI signal
cSPI2_MISO	85	IO	SPI2 SOMI signal
cSPI2_CS0	23, 83	IO	SPI2 Chip select 0 signal
cSPI2_CS2	56	IO	SPI2 Chip select 2 signal
cSPI2_CS3	54	IO	SPI2 Chip select 3 signal

ECSPI4 Signals:

Signal	Pin #	Type	Description
cSPI4_CLK	75	IO	SPI4 clock
cSPI4_MOSI	50	IO	SPI4 MOSI signal
cSPI4_MISO	77	IO	SPI4 SOMI signal
cSPI4_CS0	51, 84	IO	SPI4 Chip select 0 signal
cSPI4_CS2	56	IO	SPI4 Chip select 2 signal
cSPI4_CS3	54	IO	SPI4 Chip select 3 signal
cSPI4_RDY	57	IO	SPI4 ready signal

4.13. PCIe

VAR-SOM-SOLO/DUAL PCI Express functionality has the following parts:

PCI Express includes the following cores:

- PCI Express Dual Mode (DM) core
- PCI Express Root Complex (RC) core
- PCI Express Endpoint (EP) core

PCI Express 2.0 PHY:

- PCIe 2.0 PHY is a complete mixed-signal semiconductor intellectual property (IP) solution, designed for single-chip integration into computer applications
- The PCIe 2.0 PHY supports both the 5 Gbps data rate of the PCI Express Gen 2.0 specifications as well as being backwards compatible to the 2.5Gb/s Gen 1.1 specification

PCIE Signals:

Signal	Pin #	Type	Description
PCIE_TXP	130	DS	Positive PCI TX differential
PCIE_TXM	128	DS	Negative PCI TX differential
PCIE_RXP	134	DS	Positive PCI RX differential
PCIE_RXM	136	DS	Negative PCI RX differential
CLK1_P	102	DS	Positive PCI clock differential
CLK1_N	100	DS	Negative PCI clock differential

4.14. I²C

I2C-1, 2, 3 Interface connectivity peripherals provide serial interface for external devices. Data rates of up to 400 kbps are supported.

I2C1 Signals:

Signal	Pin #	Type	Description
I2C1_SCL	88,75	IO	I2C1 I²C clock, open drain
I2C1_SDA	87,50	IO	I2C1 I²C data, open drain

I2C2 Signals:

Signal	Pin #	Type	Description
I2C2_SCL	174	IO	I²C clock, open drain, internally PU
I2C2_SDA	176	IO	I²C data, open drain, internally PU

Note: I2C2 interface is used by PMIC, CODEC and EEPROM on-som devices (I2C ADDR =0x1B, 0x8, 0x56 & 0x57). Pin configuration for I2C2 signal can't be changed.

I2C3 Signals:

Signal	Pin #	Type	Description
I2C3_SCL	92	IO	I2C3 I²C clock, open drain
I2C3_SDA	90	IO	I2C3 I²C data, open drain

4.15. General Purpose IOs

Most of the SoM's IO pins can be used as GPIOs.
See Chapter 3, Table 3.1 and 3.2 for a complete SoM connectors signal list and GPIO multiplexing.

4.16. General System Control

4.16.1. Boot Options

Below you can find the MX6 boot options

8	7	6	5	4	3	2	1
BT_CFG1_7	BT_CFG1_6	BT_CFG1_5	BT_CFG1_4	BT_CFG2_6	BT_CFG2_5	BT_CFG2_4	BT_CFG2_3
1XXX = NANDF Boot							
011X = MMC/eMMC Boot				X0 = 1-bit X1 = 4-bit 10 = 8-bit		01 = SD2 Boot 10 = SD3 Boot 11 = SD4 Boot	
010X = SD/eSD Boot				X0 = 1-bit X1 = 4-bit		01 = SD2 Boot 10 = SD3 Boot 11 = SD4 Boot	
0011 = Serial ROM (SPINOR) Boot							
0010 = SATA Boot							

The boot-select pin configures the boot sequence of the VAR-SOM-SOLO/DUAL :
BOOT_CFG = X1X00101

Pin Name	Pin Number	MX6 BOOT_CFG	Internally pulled
BOOT_SEL0	42	BT_CFG1_7	Pulled-up 10K
BOOT_SEL1	40	BT_CFG1_5	Pulled-down 10K

Use cases:
BOOT_SEL [1:0] = [0:1] => BOOT_CFG = 11000101 => NAND Boot
BOOT_SEL [1:0] = [0:0] => BOOT_CFG = 01000101 => SD2 boot, SD-Card, 4 bit bus
BOOT_SEL [1:0] = [1:0] => BOOT_CFG = 01100101 => SD2 boot, eMMC (external, on carrier board) ,4 bit bus
Note: boot from on-SOM eMMC is not possible

4.16.2. Reset

'0' logic will reset VAR-SOM-SOLO/DUAL

A Delay should be added on POR_B to ensure POR_B is released after SOM voltage rails have stabilized. Use a voltage supervisor, see reference schematics.

4.16.3. Reference Clock Out

VAR-SOM-SOLO/DUAL output clock (CLKO2) is controlled by the i.MX6 CCM module. Please refer to the i.MX6 user manual regarding the configuration option for this clock.

4.16.4. General System Control Signals

Signal	Pin #	Type	Description
CLKO	29	O	Clock out
BOOT_SEL0	42	I	Refer to section 4.19.1
BOOT_SEL1	40	I	Refer to section 4.19.1
POR_B	98	I	Hardware reset

4.17. Power

4.17.1. Power Supply

Signal	Pin #	Type	Description
VIN_3V3	32, 34, 36, 38, 103, 105, 107, 109, 111	Power In	VAR-SOM-SOLO/DUAL Single DC-IN Supply voltage. Voltage range: 3.3 +/- 5%
3V3_PER	49	Power Out	3.3 V output, up to 200 mA

4.17.2. Ground

Signal	Pin #	Type	Description
GND	13, 14, 19, 27, 28, 31, 33, 35, 37, 47, 58, 59, 66, 67, 76, 78, 89, 95, 101, 112, 118, 126, 132, 138, 139, 144, 149, 158, 159, 169, 172, 178, 179, 185	Power	Digital ground
AGND	195,196	Power	Audio analog GND

5. Absolute Maximum Characteristics

Power Supply	Min	Max	Unit
Main Power Supply, DC-IN	-0.3	3.5	V

6. Operational Characteristics

6.1. Power supplies

	Min	Typical	Max	Unit
Main Power Supply, DC-IN	-5%	3.3	+5%	V

6.2. Power Consumption

CPU usage:

Task	SOM VBAT current draw in ma @3.3v
Idle (~10% CPU) @ 400mhz	330mA
FHD Video playback	650mA

Additional peripherals:

Task	SOM VBAT current draw in ma @3.3v
WLAN transmission 2.4Ghz 802.11(b/g/n)	~(460-530)mA
WLAN transmission 5Ghz 802.11(a)	~540mA
Gbit Ethernet	~610mA

7. DC Electrical Characteristics

Parameter	Min	Typical	Max	Unit
Digital 3.3V				
V_{IH}	0.7x VIN_3V3		VIN_3V3	V
V_{IL}	0		0.3x VIN_3V3	V
V_{OH}	VIN_3V3- 0.15			V
V_{OL}			0.15	V

Table 7-1 DC Electrical Characteristics

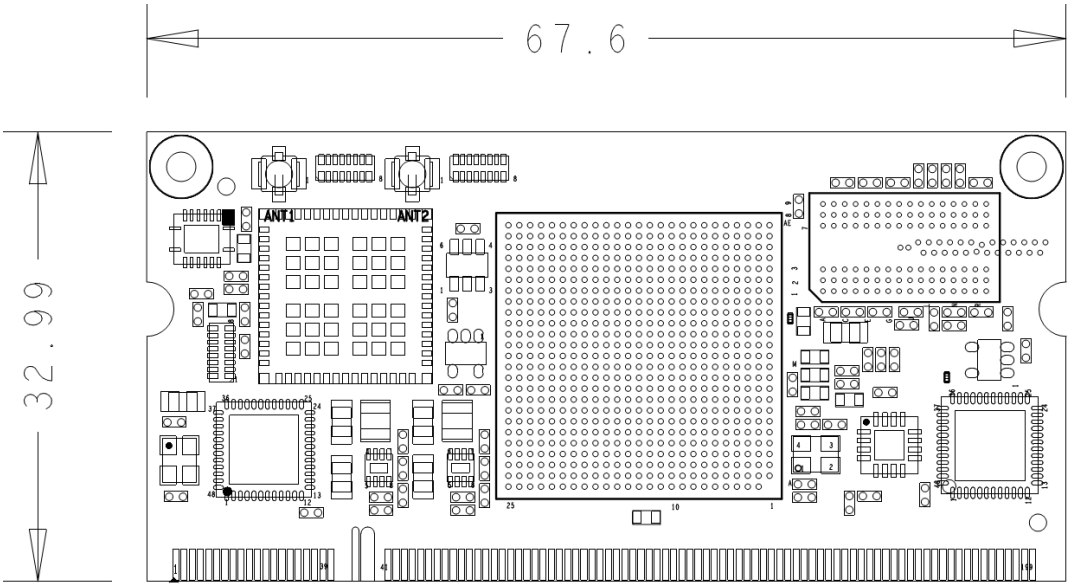
8. Environmental Specifications

	Min	Max
Commercial Operating Temperature Range	0 ^{0}C	+70 ^{0}C
Extended Operating Temperature Range	-20 ^{0}C	+70 ^{0}C
Industrial Operating Temperature Range	-40 ^{0}C	+85 ^{0}C
Storage temperature	-40°C	85°C
Relative humidity (operation)	10%	90%
Relative humidity (storage)	05%	95%
Referring MIL-HDBK-217F-2 Parts Count Reliability Prediction Method Model: 25Deg Celsius, Class B-1, GM 25Deg Celsius, Class B-1, GF 25Deg Celsius, Class B-1, GB	 374 Khrs > 823 Khrs > 2600 Khrs >	

Note: Extended and Industrial Temperature is only based on the operating temperature grade of the SoM components. Customer should consider specific thermal design for the final product based upon the specific environmental and operational conditions.

9. Mechanical Drawings

Top View [mm]



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