

Symphony-Board



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#### Disclaimer:

Schematics are for reference only.  
Variscite LTD provides no warranty for the use of these schematics.  
Schematics are subject to change without notice.

#### Revision History

| Document | Carrier |   |
|----------|---------|---|
| 1.0      | 1.0     | Initial   |
| 1.1      | 1.1     | Released  |
| 1.2      | 1.1     | Updated Block Diagrams<br>Added SH1 wire short symbol<br>Updated Compatibility value for SOM pins 68,69,176<br>Updated SOM pin 22 net name<br>Fixed U22,B1, C113,1 net name<br>Fixed R1-R2,R35-R38 net name   |
| 1.3      | 1.2     | Removed SH1 wire short, J1.68 routed to capacitive touch<br>Changed R29 to C185<br>Changed R123,R127 to N.C.<br>Added resistors R130-132<br>Removed ADC_INxx alternate function from VAR-SOM-MX8 Symbol<br>Updated PCIe resistor assembly note  |
| 1.4      | 1.2     | Updated Parallel Camera/HDMI/DP Note<br>Fixed ETH pin names VAR-SOM-MX8X Symbol   |
| 1.5      | 1.2A    | Disconnected R129   |
| 1.6      | 1.2A    | Added VAR-SOM-MX8M-MINI Block Diagram and Symbol<br>PRE-RELEASE VERSION!!!! Subject to change without notice  |
| 1.7      | 1.2B    | Fixed VAR-SOM-MX8M-MINI Symbol<br>Changed U29,U30,U31 to P/N: PPF2193<br>Changed R60 to 47K   |
| 1.8      | 1.2C    | Update VAR-SOM-MX8M-MINI Symbol to V1.1 with side notes for v1.0B(Early access customers)<br>Update VAR-SOM-MX8M-MINI Block Diagram<br>POR circuitry fed by VCC_SOM: see U7 R60 R61 R40 R60<br>D5 Removed   |
| 1.9      | 1.2D    | Raise VCC_3V3 to Nominal 3.39V for VAR-SOM-MX8M-MINI/NANO<br>power up threshold voltage requirement of >3.35V   |
| 1.10     | 1.2E    | Reference for new designs: (changes not implemented in V1.2 BRD)<br>* Added x2 studs for heat plate support<br>* Base_per_3v3 added slew rate limit<br>* U7 (Base POR circuit) added CB_WDOG resistor assembly options<br>* U29 U30 U31 - Added assembly note<br>* VAR-SOM-MX8M-NANO pages added with symbol pinout<br>* VAR-SOM-MX8 Connector update - added NC on /? assembly options<br>* Power switch in OFF position discharge of Custom rails added<br>* Ethernet magnetics - support two Marf: Pulse & UDE;<br>* Base RJ45 LEDs matched to SOM behaviour;  |
| 1.11     | 1.3     | * Added VAR-SOM-MX8M-PLUS Preliminary Symbol and Block Diagram<br>Symbol is Pre-Release Version! Subject to change without notice!<br>* All C1210 capacitor footprint updated to C1210_v0<br>* MS1 to MS6 not assembled   |
| 1.12     | 1.3A    | * ETH1 PHY clock filter U9 replaced with 49.5 Ohm /0603 resistor<br>* Added design note for ETH1 switches U8 and U10.   |
| 1.13     | 1.4     | * MS5 and MS6 location adopted to heatplate design - Layout<br>* Update J1 Manufacturer P/N, NAME and footprint to represent the assembled part<br>* Replace PCIe AC caps on RX lines with 0 ohm resistors<br>* Updated VAR-SOM-MX8M-PLUS Symbol pins 1 58 80, swap pins 41 43 and 84 147<br>* J19 Modify Camera connector orientation<br>* Remove U8 U10 analog switches on ETH1<br>* U9 revert to EMI filter on RGMII_RX clock line<br>* Added RN1 RN2 RN3 R151 R136 isolating stubs on ETH1 RGMII signals<br>* U26 footprint updated to DS<br>* Y1 C68 C67 updated<br>* Support for VAR-SOM-6UL boot:<br>- BOOT_MODE1 - R117 assembled<br>- BOOT_MODE0 - Added PD R149<br>- USB&A PWR to HOST J23 always enabled<br>* Remove R39 on pin J1-156 to support SOM-MX8MP 2nd MIPI-CSI Lane2 routing<br>* J3 J30 pinout change |
| 1.14     | 1.4A    | * Support for VAR-SOM-MX8MP USB OTG -<br>Changed U5,P4 Pull for board identification, U21.9 connected to GPIO:<br>- Changed R43,R130,R106 to N.C.<br>- Changed R44,R132 to Assembled<br><br>* Changed Q4 P/N from: TPS27082L (EOL) to -> TPS27081A<br>* Updated VAR-SOM-MX8M-PLUS Block Diagram, Symbol pins 36,38 names<br>* Added notes for SOM pins 29,79,84   |
| 1.15     | 1.4A    | Changes in v1.14/1.4A for R43,R44 were not implemented (part of board identification)<br>and only appear in revision history; board identification implemented via EEPROM U3.<br>Board identification required for OS to identify method of OTG ID used: PTN5150 or GPIO  |
| 1.16     | 1.5     | * Modified VCC_3V3 to 3.35V nominal for all SOMs.<br>For VAR-SOM-MX8M-MINI/NANO, power up threshold voltage requirement of >3.35V<br>is implemented using Q10,R152<br><br>* Added note for VAR-SOM-MX8M-MINI/NANO pin 91  |
| 1.17     | 1.5     | * Updated note for I2C#B pull up resistors  |
| 1.18     | 1.5     | * Updated note for PTN36043BXY chip   |
| 1.19     | 1.5A    | * Q10 changed to 2N7002P-215<br>Transistor Q10 changed to 2N7002P to stabilize the SOM voltage in the OFF state.<br>Old transistor leakage current (IDG) changed the feedback current and increased<br>the SOM voltage.<br>2N7002P does not have SG diode that allowed IDSS to flow into the Gate<br><br>* SOM Pin 84 Note changed  |
| 1.20     | 1.6     | Ethernet PHY replaced to ADIN1300<br>R22,R23,R35,R36 assembled with Ferrite Bead<br>C185 assembled with 10K resistor, R30 not assembled<br>U2 changed to CRTL02043B<br>USB3 crossover switch changed to CRTL02043B  |
| 1.21     | 1.6A    | Due to EOL: U35 changed to NFL18ZT207H1A3D<br>Due to allocation problems: U13 changed to SN65HVD232QDR  |
| 1.22     | 1.6B    | Due to allocation problems: U22,U29,U30,U31 changed to P/N: PPF2194   |
| 1.23     | 1.6C    | Added VAR-SOM-AM62 Block Diagram and Symbol<br>Added VAR-SOM-MX93 Block Diagram and Symbol<br>Temporary removed compatibility notes<br>Added hand wired EXP_MDIO_EN line.   |



### 03.SOM

#### OFF PAGE CONNECTOR INDEX:

1. Function# :Interface common to ALL SOMs
2. J1.xxx-Function :Interface common to certain SOMs or Used for carrier board common function
3. J1.xxx :No common interface

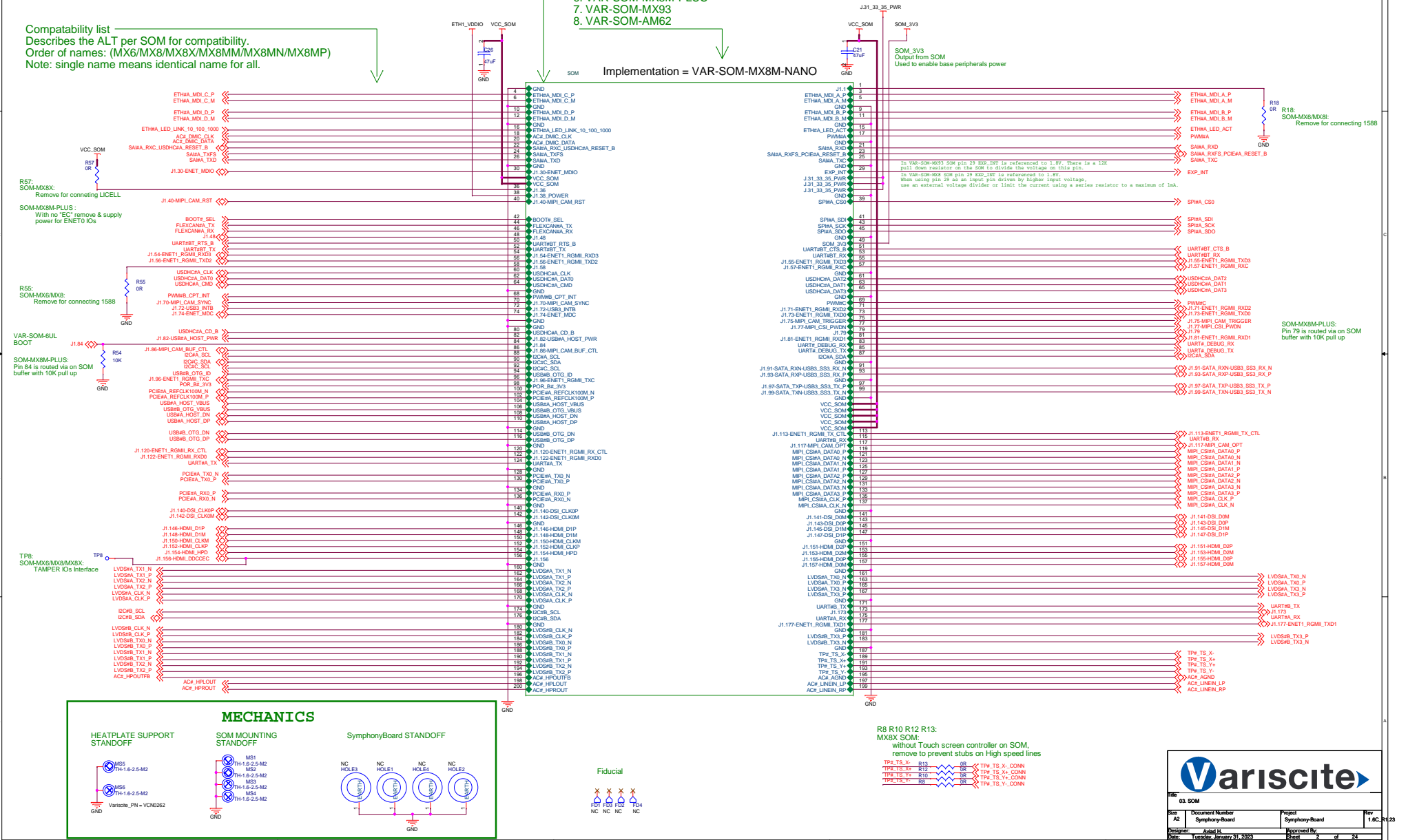
#### Compatibility list

Describes the ALT per SOM for compatibility.  
Order of names: (MX6/MX8/MX8X/MX8MM/MX8MN/MX8MP)  
Note: single name means identical name for all.

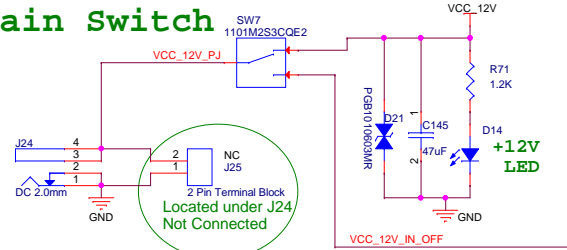
For cross probing between SOM symbol and the specific SOM Connector used,  
set the "Implementation" property value in SOM port symbol  
to one of the following:

1. VAR-SOM-MX6
2. VAR-SOM-MX8
3. VAR-SOM-MX8X
4. VAR-SOM-MX8M-MINI
5. VAR-SOM-MX8M-NANO
6. VAR-SOM-MX8M-PLUS
7. VAR-SOM-MX93
8. VAR-SOM-AM62

For complete alternate function per pin and specific SOM:  
please refer to "VAR-SOMs Compatibility and Pinout.XLS " located at:  
[ftp://ftp.variscite.com/SOM\\_Compatibility](ftp://ftp.variscite.com/SOM_Compatibility)



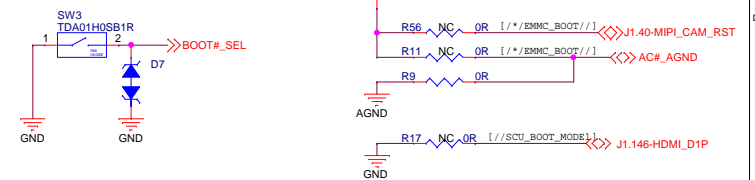
## 12VDC INPUT Main Switch



```

Boot Options:
OFF : INT
ON  : SD
Internal boot is from eMMC
MX6 for eMMC boot see additional changes note

```



The diagram shows a 5V/8A power supply module. The input is VCC\_12V, which is connected to the VIN pin of the U18 RT2999BHGQW converter. The output is VCC\_5V, which is connected to the 5V pin of the module. A +5V LED (D13) is connected to the 5V output. The circuit includes various capacitors (C99, C100, C79, C102, C101, C78, C82, C83, C84, C103, C104) and resistors (R81, R75, R82, R83, R70) for filtering and regulation. The U18 RT2999BHGQW converter is the central component, with pins for VIN, BOOT, PVIN, PVIN-, PGOOD, COMP, GND, and SS/TR. The output is connected to the 5V pin of the module, which is also connected to the +5V LED.

**3.35V/8A FROM PWR JACK**

**SOM SOM PWR**

**SOM CURRENT MEASURING:**  
REMOVE R58 AND CONNECT SERIES AMPERMETER

**Note:**  
VAR-SOM-MX6M-MINI/NANO:  
VCC\_SOM when rising  
must be > 3.35V for  
the SOM to power up.  
Set to nominal 3.44V

Note for U29:  
Recommended PM for redesign: FPF2193  
Assembled board can have FPF2194.

D24: PIN 31 33 35  
FAULT LED

VCC\_3V3

VCC\_SOM

R119 10K

PINS\_31\_33\_35

PWR\_EN

D23

TDA01H0SB1R

SW6

C158 10uF

C2

U29 FPF2194

B2 A2

Vin EN

Vout FLAG

GND Iset

C1

R120 365R 1% 100nF

C159

R121 221R 1%

D24

J.31\_33\_35

PWR

Switch defaults to OFF,  
Must be set to ON when connecting  
MX6 based SOMs

**RTC BATTERY**

BASE\_PER\_3V3

D15

BAT54CLT1G

RTC\_IN

FB6

VCC\_RTC

C89

C88

120R 1.2A

22uF

100nF

GND

I2C ADD:0x68/R/W

U20

DS1337U+

Vcc

XI

Fout

XO

IRQ2#

SDA

SCL

GND

XI

XO

Y2

32.768KHz

COIN\_IN

R108

1.47K 1%

JBT1

CR1225-HOLDER

BASE\_PER\_3V3

BASE\_PER\_3V3

I2C#0\_SDA

I2C#0\_SCL

**BOARD ID**

U3

BR24G04NUX-3TTR

A0

A1

A2

VSS

VCC

WP

SCI

SDA

GND

'1' = WP

ADD= 0x33

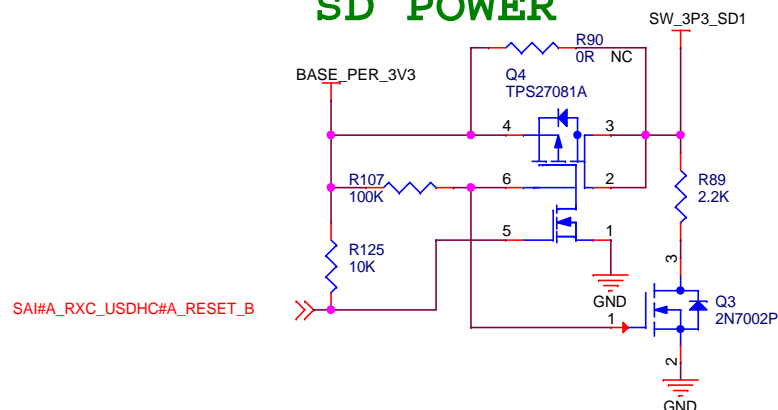
Address 0x54,0x55

[illegible]

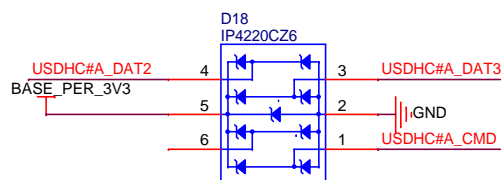
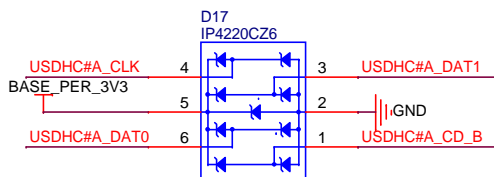
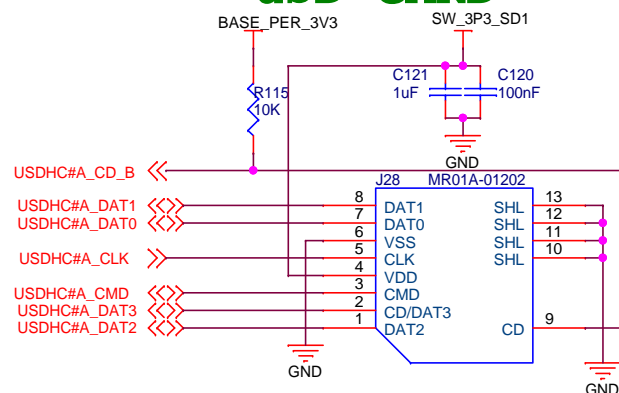
|                                |                 |               |                   |
|--------------------------------|-----------------|---------------|-------------------|
| Size<br>A3                     | Document Number | Project       | Rev<br>1.6C_R1.23 |
| Designer: Aviad H.             |                 | Approved By:  |                   |
| Date: Monday, January 30, 2023 |                 | Sheet 3 of 24 |                   |

## 06. *uSD, Audio, CAN*

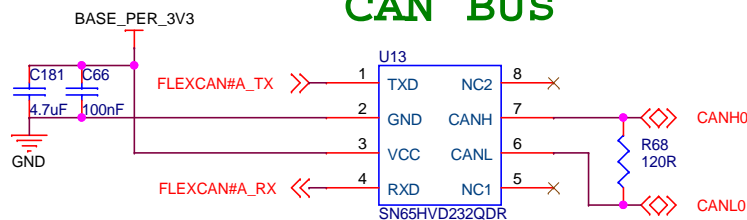
## SD POWER



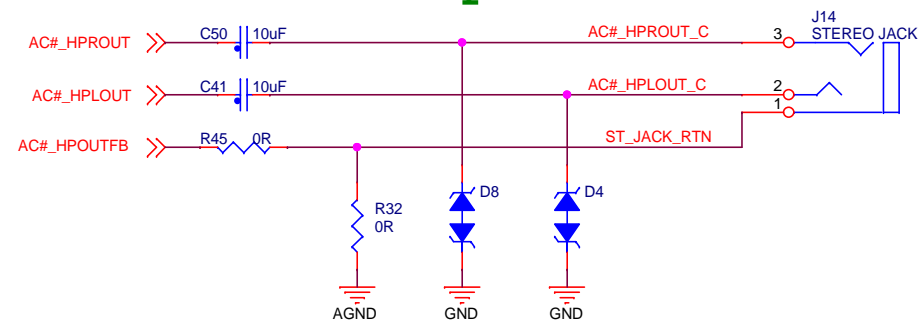
## USD CARD



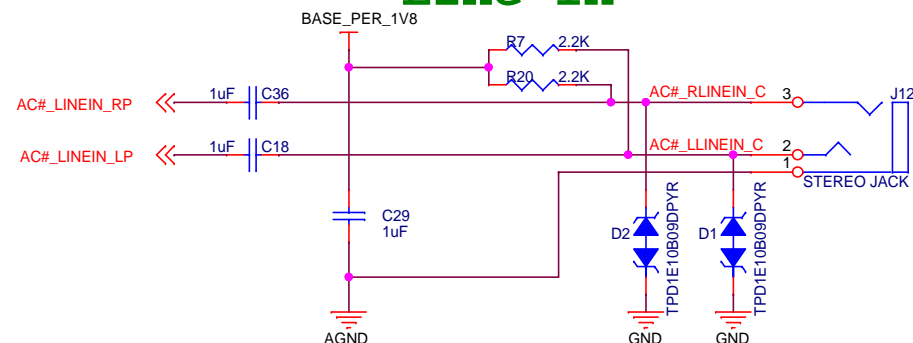
# CAN BUS



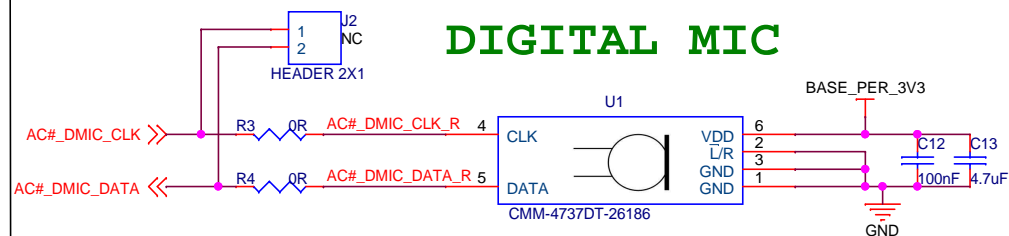
## Headphones



## Line In

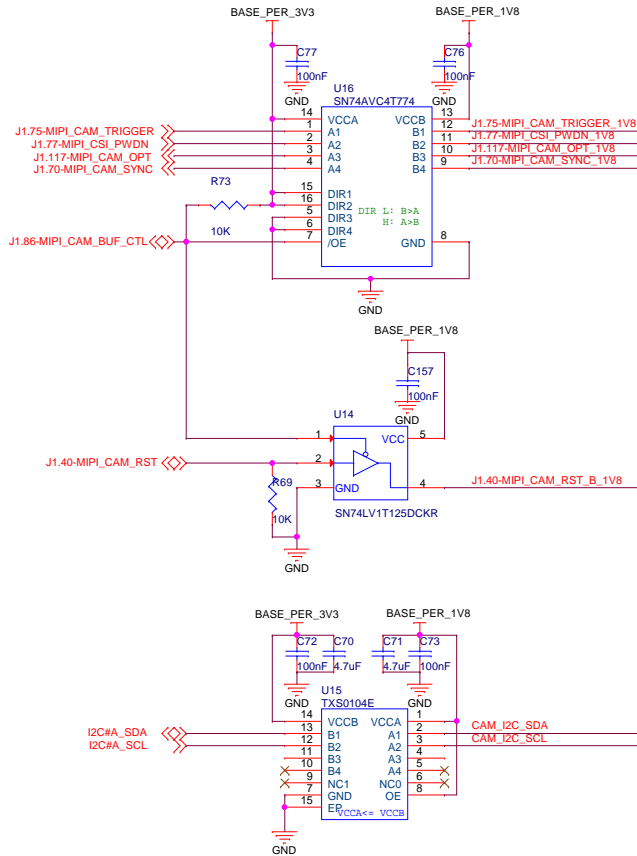


## DIGITAL MIC

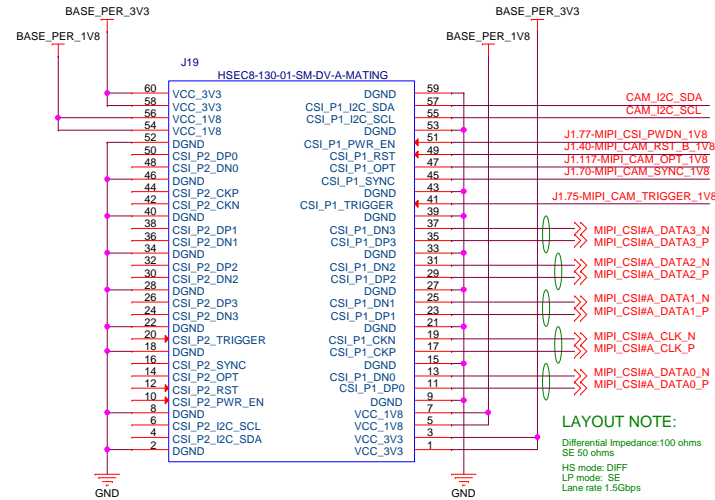


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|---|-----------------------------------|-------------------------------|------------------|
| Title                                       |                                   |                               |                  |
| 06. uSD, Audio, CAN                         |                                   |                               |                  |
| Size<br>A4                                  | Document Number<br>Symphony-Board | Project<br>Symphony-Board     | Rev<br>1.6C R1.2 |
| Designer:<br>Date: Monday, January 30, 2023 |                                   | Approved By:<br>Sheet 4 of 24 |                  |

# 07. Camera, HDMI, DP



## MIPI-CSI



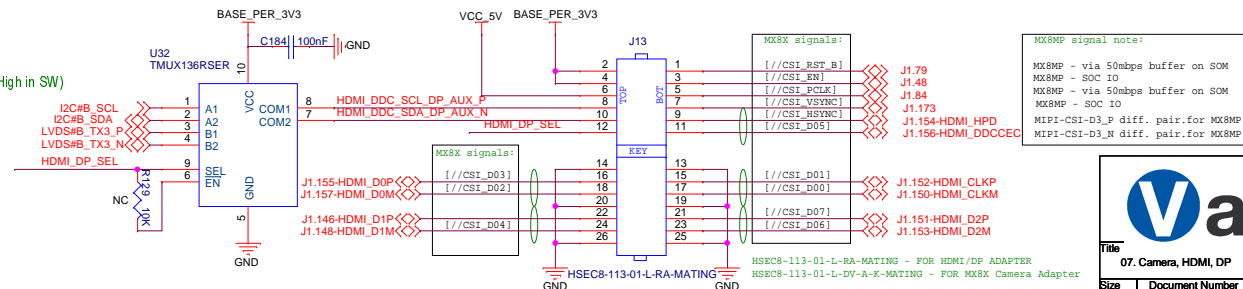
Note:  
MIPI\_CSI#A signals appears on bottom side of J19  
as of SymphonyBoard V1.4.

## J13: MX6/MX8-HDMI, MX8-DP, MX8X-CSI, MX8MP-2nd MIPI-CSI

Note for U32 (analog switch):  
Switch is to enable support for the following adapters:  
Parallel camera, HDMI, DisplayPort and second MIPI-CSI.

- Switch select controlled on adaptor will select between:  
1) I2C#B which can export  
VAR-SOM-MX8X: I2C3 Used by parallel camera  
VAR-SOM-MX8: HDMI DDC Used by HDMI (GPIO1\_22 in should be set High in SW)  
2) LVD#B\_TX3 which can export:  
VAR-SOM-MX8(DP assembly option): HDMI AUX used by DP

Switch can be omitted when designing for only one of the above interfaces.



## 08. Ethernet

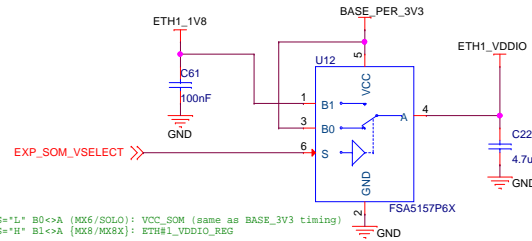
### Header/Stub isolation resistors

|                           |                    |    |          |      |            |
|---------------------------|--------------------|----|----------|------|------------|
| J1.54-ENET1_RGMII_RXD3    | ENET1_RGMII_RXD3   | NC | R173     | 0R   | J1.54_EXT  |
| J1.71-ENET1_RGMII_RXD2    | ENET1_RGMII_RXD2   | NC | R174     | 0R   | J1.71_EXT  |
| J1.122-ENET1_RGMII_RXD0   | ENET1_RGMII_RXD0   | NC | R175     | 0R   | J1.122_EXT |
| J1.81-ENET1_RGMII_RXD1    | ENET1_RGMII_RXD1   | NC | R176     | 0R   | J1.81_EXT  |
| J1.120-ENET1_RGMII_RX_CTL | ENET1_RGMII_RX_CTL | NC | 49.9R 1% | R151 | J1.120_EXT |
| J1.57-ENET1_RGMII_RXC     | ENET1_RGMII_RXC    | NC | 1.0K 1%  | R136 | J1.57_EXT  |
| J1.113-ENET1_RGMII_TX_CTL | ENET1_RGMII_TX_CTL | NC | R179     | 0R   | J1.113_EXT |
| J1.96-ENET1_RGMII_TXC     | ENET1_RGMII_TXC    | NC | R180     | 0R   | J1.96_EXT  |
| J1.73-ENET1_RGMII_TXD0    | ENET1_RGMII_TXD0   | NC | R181     | 0R   | J1.73_EXT  |
| J1.177-ENET1_RGMII_TXD1   | ENET1_RGMII_TXD1   | NC | R182     | 0R   | J1.177_EXT |
| J1.56-ENET1_RGMII_TXD2    | ENET1_RGMII_TXD2   | NC | R177     | 0R   | J1.56_EXT  |
| J1.55-ENET1_RGMII_TXD3    | ENET1_RGMII_TXD3   | NC | R178     | 0R   | J1.55_EXT  |

Note:  
Customer requiring usage of J30 header (located on bottom side)  
should assemble these resistors if not assembled by default

### VDD\_ENET for SOM-MX8/MX8X/MX8MP

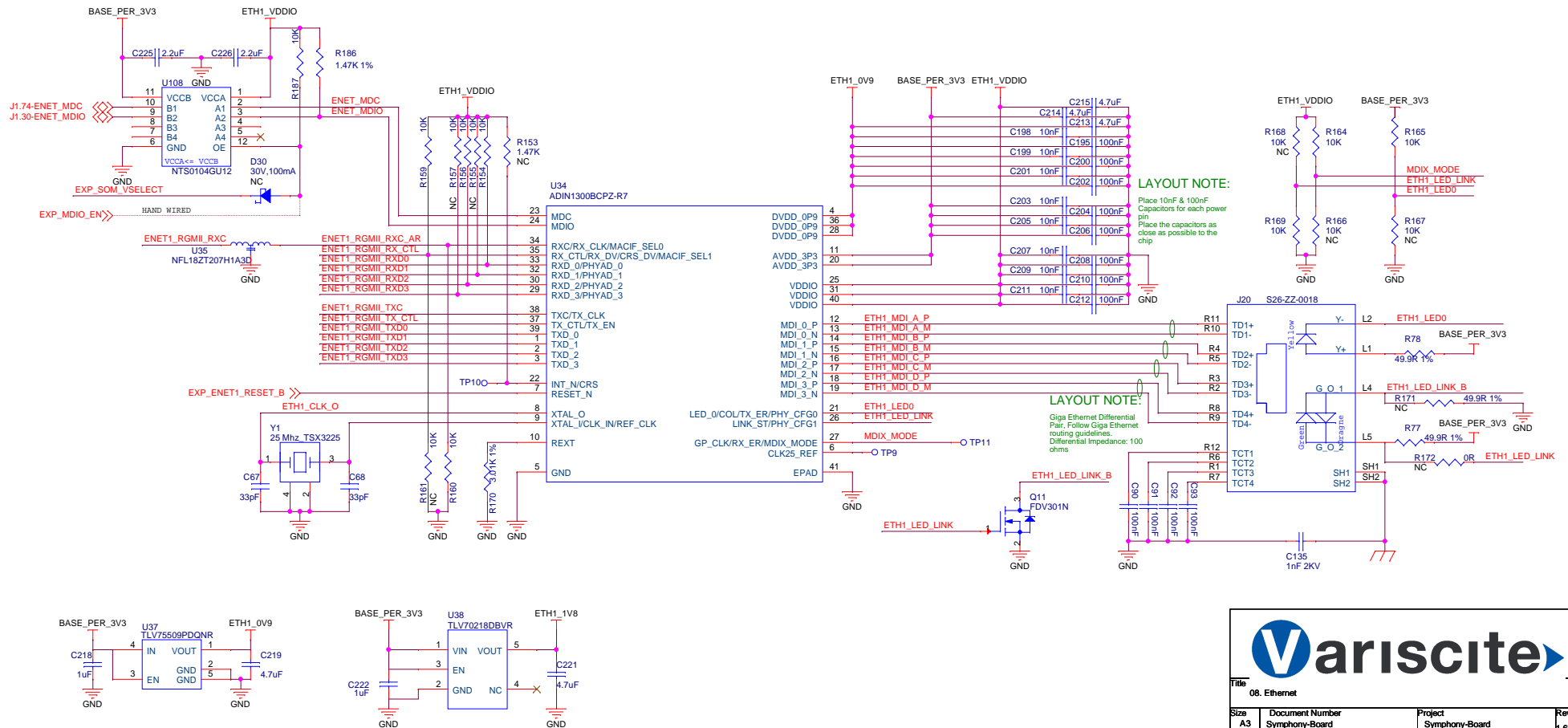
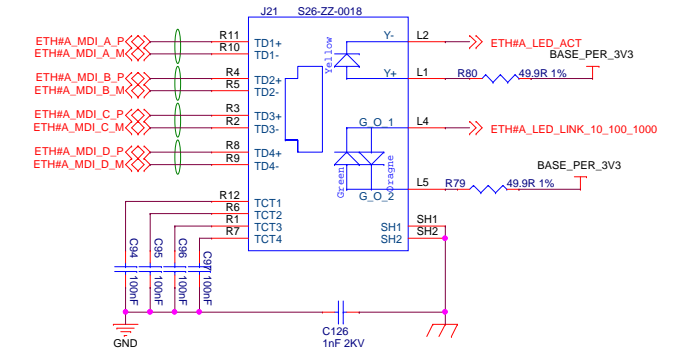
Power for ENET1\_RGMII IOs on SOM power fed from pin J1.38  
For specific SOM listed above, requiring second ETH port on ENET1 this power should be set to 1.8V source from U11 PHY



S="L" B0<A {MX8/SOLO}: VCC\_SOM (same as BASE\_3V3 timing)  
S="H" B1<A {MX8/MX8X}: ETH1\_VDDIO\_REG

## Gigabit Ethernet (Internal)

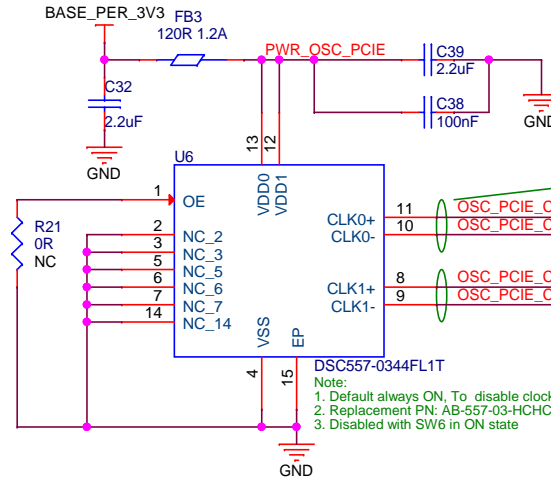
LAYOUT NOTE:  
Giga Ethernet Differential Pair,  
Follow Giga Ethernet routing  
guidelines.  
Differential Impedance: 100 ohms



|                                  |                                   |                           |                   |
|----------------------------------|-----------------------------------|---------------------------|-------------------|
| Title<br>08. Ethernet            |                                   |                           |                   |
| Size<br>A3                       | Document Number<br>Symphony-Board | Project<br>Symphony-Board | Rev<br>1.6C_R1.23 |
| Designer<br>Aviad H.             | Approved By                       |                           |                   |
| Date<br>Monday, January 30, 2023 | Sheet<br>6                        | of<br>24                  |                   |

# 09. PCIe

## PCIe CLK



### LAYOUT NOTE:

Differential Impedance:  
100 ohms

PCIE#A\_REFCLK100M\_P  
PCIE#A\_REFCLK100M\_N

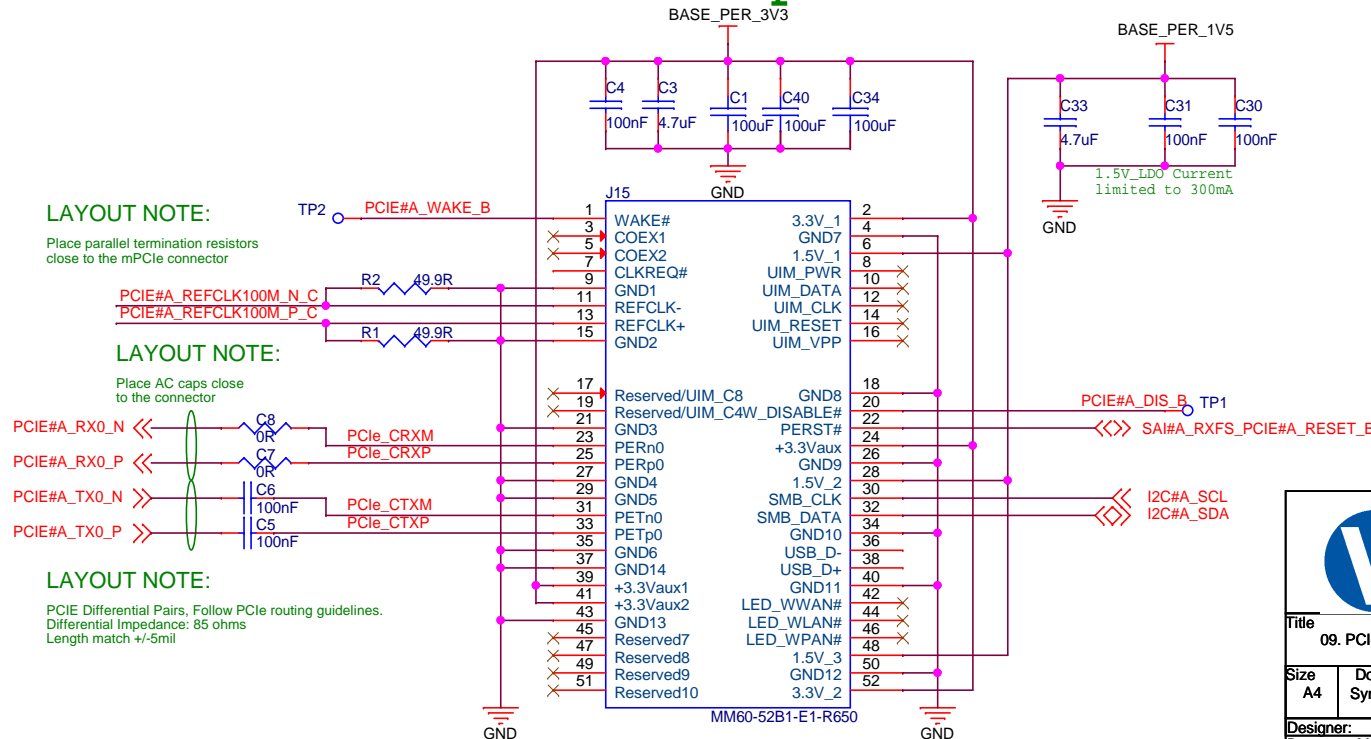
PCIE#A\_REFCLK100M\_P\_C  
PCIE#A\_REFCLK100M\_N\_C

SOM-6UL NAND  
signals should  
not be driven

### LAYOUT NOTE:

Place parallel termination resistors  
as close to the SOM connector  
as possible.

## mPCIexp



### LAYOUT NOTE:

Place parallel termination resistors  
close to the mPCIe connector

### LAYOUT NOTE:

Place AC caps close  
to the connector

### LAYOUT NOTE:

PCIe Differential Pairs, Follow PCIe routing guidelines.  
Differential Impedance: 85 ohms  
Length match +/-5mil

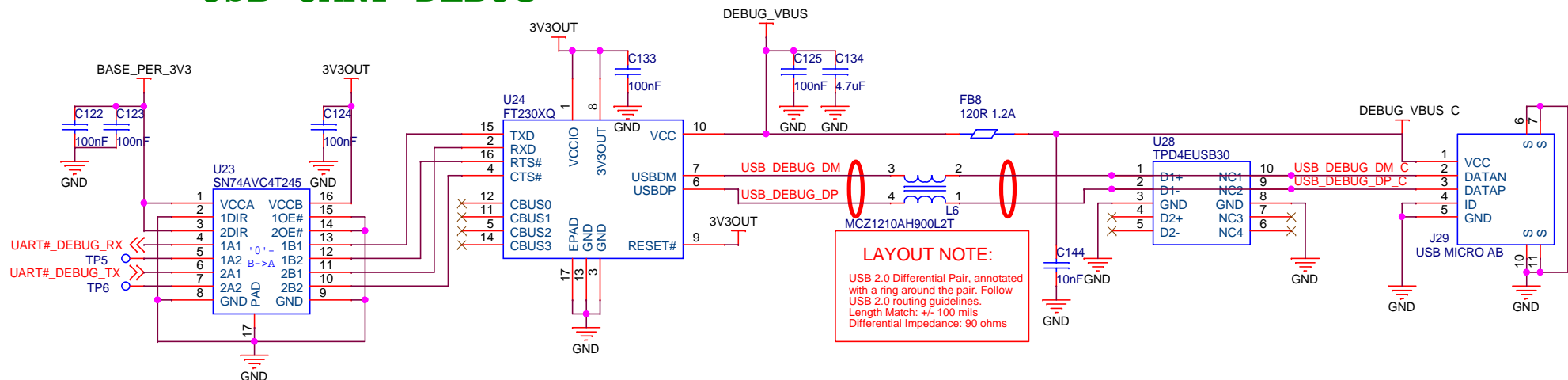


|   |                                   |                               |                   |
|---|-----------------------------------|-------------------------------|-------------------|
| Title<br>09. PCIe                           |                                   |                               |                   |
| Size<br>A4                                  | Document Number<br>Symphony-Board | Project                       | Rev<br>1.6C_R1.23 |
| Designer:<br>Date: Monday, January 30, 2023 |                                   | Approved By:<br>Sheet 7 of 24 |                   |

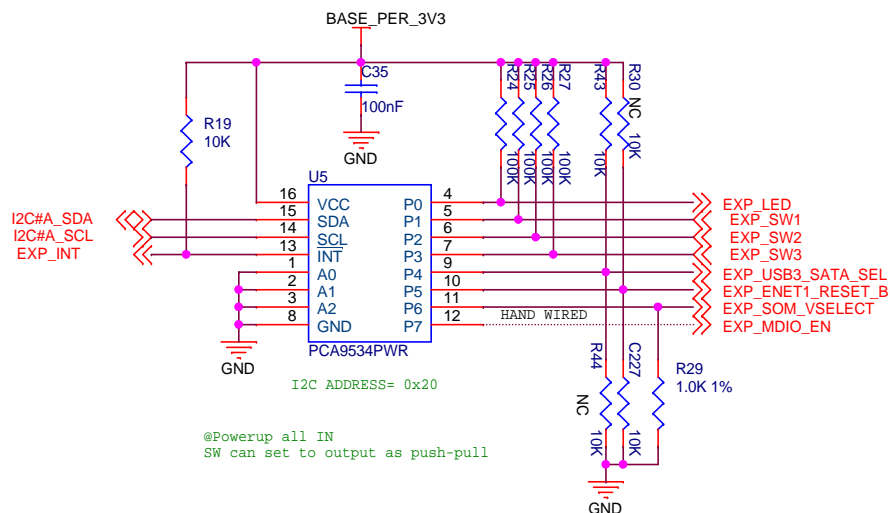


# 10. Debug, GPIO Exp, Buttons, LED

## USB UART DEBUG

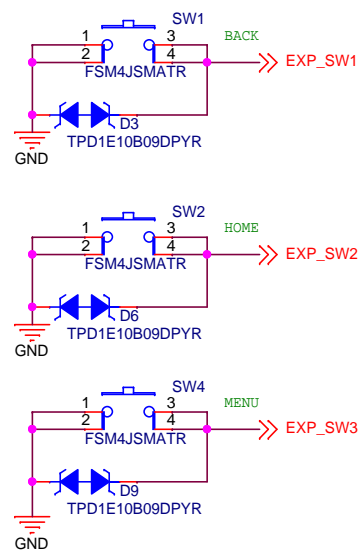


## GPIO EXPANDER



In VAR-SOM-MX8 SOM pin 29 EXP\_INT is referenced to 1.8V.  
When using pin 29 as an input pin driven by higher input voltage,  
use an external voltage divider or limit the current using a series resistor to a maximum of 1mA.

## GP BUTTON



## GP LED

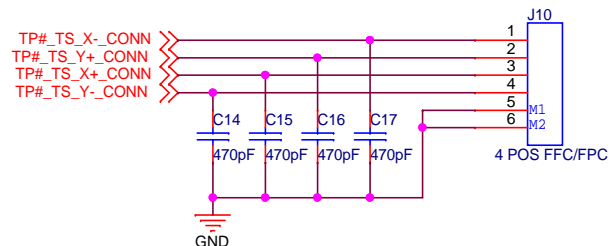


|  |                                   |                               |                   |
|--|-----------------------------------|-------------------------------|-------------------|
| Title<br>10. Debug, GPIO Exp, Buttons, LED |                                   |                               |                   |
| Size<br>A4                                 | Document Number<br>Symphony-Board | Project                       | Rev<br>1.6C_R1.23 |
| Designer:<br>Monday, January 30, 2023      |                                   | Approved By:<br>Sheet 8 of 24 |                   |

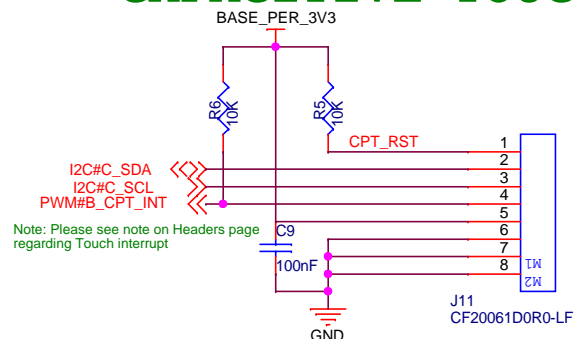


# 11. LVDS, DSI, Touch

## RESISTIVE TOUCH



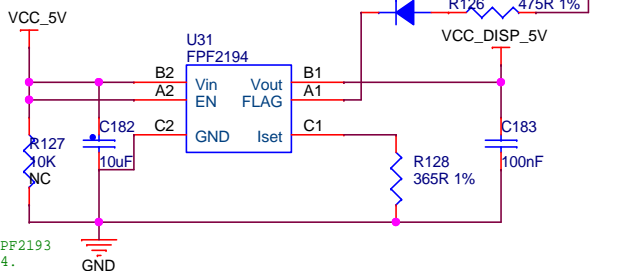
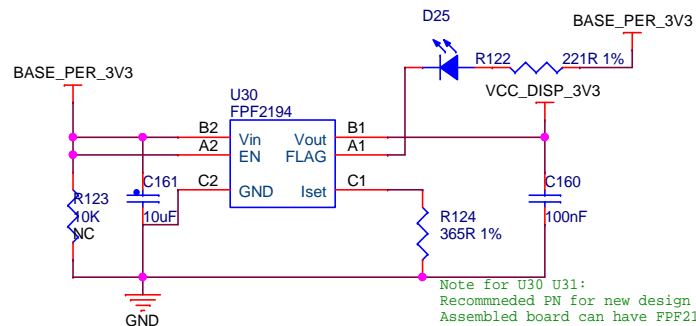
## CAPACITIVE TOUCH



See note in :  
"Headers" Page 14

J1.57\_EXT <<>  
CB\_WDOG\_B >>  
J1.82-USB#A\_HOST\_PWR >>  
CB-USB#A\_HOST\_PWR >>

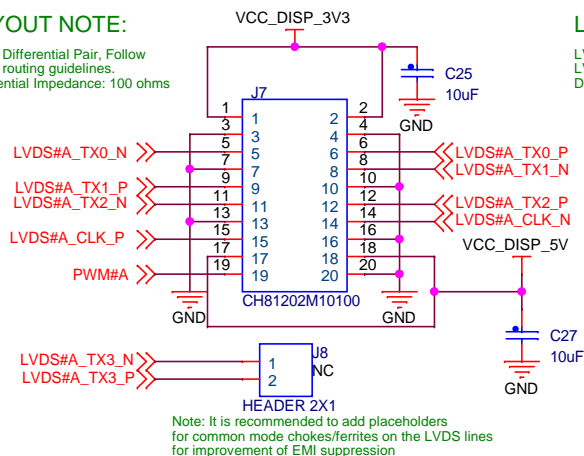
## Short circuit protection



## LVDS DISPLAY A

### LAYOUT NOTE:

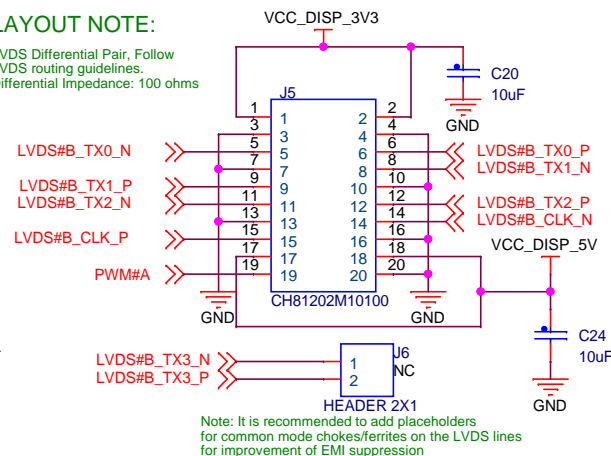
LVDS Differential Pair, Follow  
LVDS routing guidelines.  
Differential Impedance: 100 ohms



## LVDS DISPLAY B

### LAYOUT NOTE:

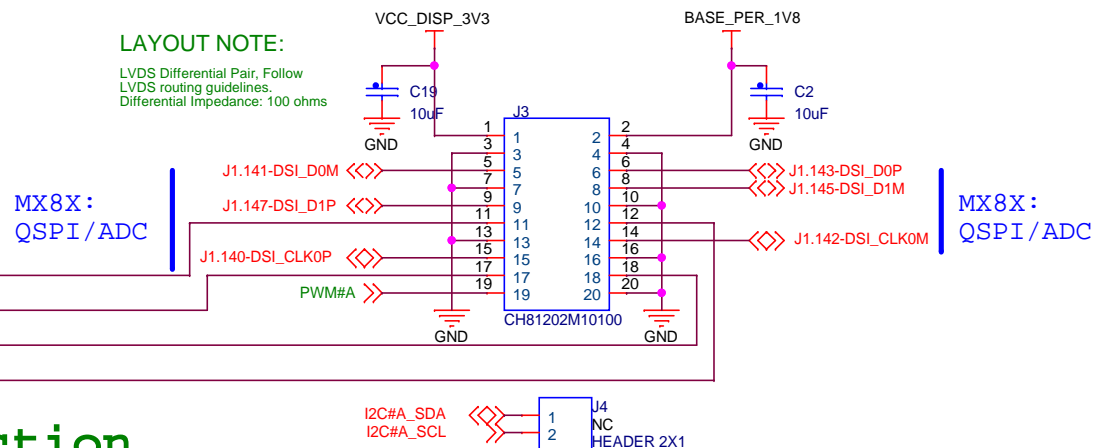
LVDS Differential Pair, Follow  
LVDS routing guidelines.  
Differential Impedance: 100 ohms



## MIPI DSI DISPLAY

### LAYOUT NOTE:

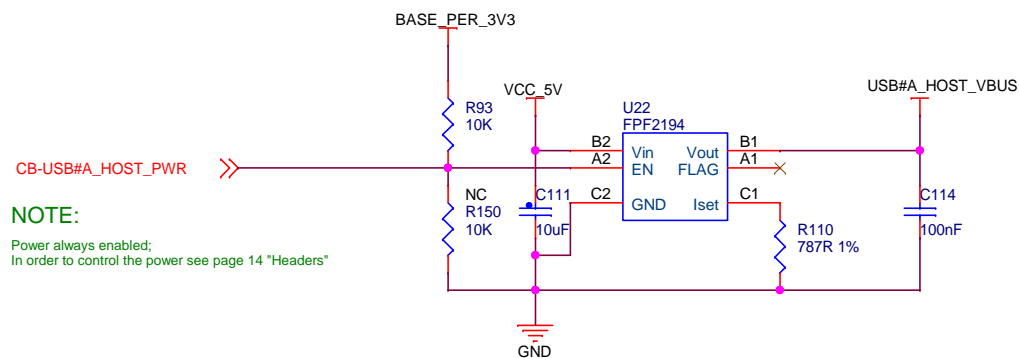
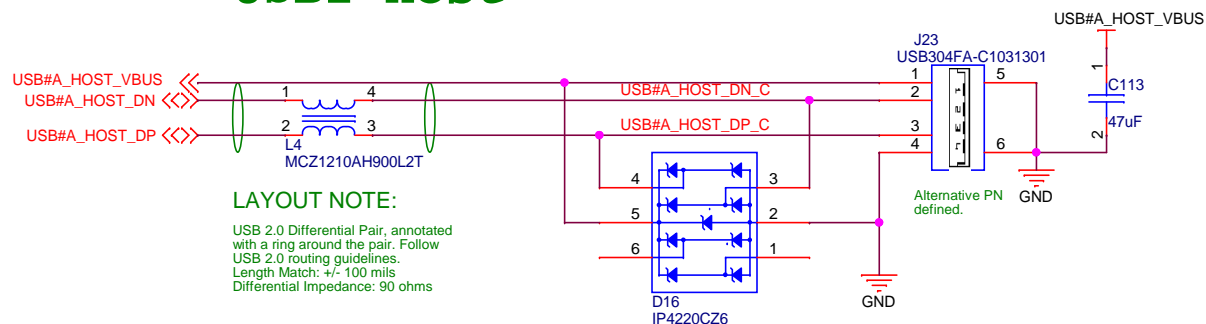
LVDS Differential Pair, Follow  
LVDS routing guidelines.  
Differential Impedance: 100 ohms



|                                       |                                   |                               |                  |
|---------------------------------------|-----------------------------------|-------------------------------|------------------|
| Title<br>11. LVDS, DSI, Touch         |                                   |                               |                  |
| Size<br>A4                            | Document Number<br>Symphony-Board | Project<br>Symphony-Board     | Rev<br>1.6C R1.2 |
| Designer:<br>Monday, January 30, 2023 |                                   | Approved By:<br>Sheet 9 of 24 |                  |

# 12. USB2 Host

## USB2 Host



|                                       |                                   |                                |             |
|---------------------------------------|-----------------------------------|--------------------------------|-------------|
| Title<br>12. USB2 Host                |                                   |                                |             |
| Size<br>A4                            | Document Number<br>Symphony-Board | Project<br>Symphony-Board      | Rev<br>1.6C |
| Designer:<br>Monday, January 30, 2023 |                                   | Approved By:<br>Sheet 10 of 24 |             |

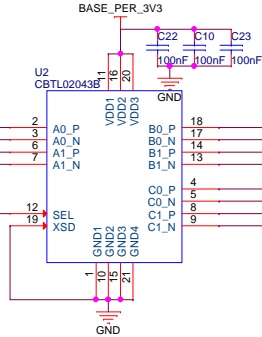
## 13. USB3, uSATA

### SATA/USB select

J1.93-SATA\_RXP-USB3\_SS3\_RX\_P  
J1.91-SATA\_RXN-USB3\_SS3\_RX\_N  
J1.97-SATA\_TXP-USB3\_SS3\_TX\_P  
J1.99-SATA\_TXN-USB3\_SS3\_TX\_N

EXP\_USB3\_SATA\_SEL >>

SEL = LOW: A <-> B  
SEL = HIGH: A <-> C  
XSD = LOW: ON  
XSD = HIGH: OFF  
By default, lines routed to SATA



#### LAYOUT NOTE:

USB 3.0 Differential Pair, annotated with a ring around the pair. Follow USB 3.0 routing guidelines. Differential Impedance: 85 ohms

USB3\_SS3\_RX\_P  
USB3\_SS3\_RX\_N  
USB3\_SS3\_TX\_P  
USB3\_SS3\_TX\_N

SATA\_RXP  
SATA\_RXN  
SATA\_TXP  
SATA\_TXN

#### LAYOUT NOTE:

SATA Differential Pair, Follow SATA routing guidelines. Differential Impedance: 85 ohms Length match +/-5mil

### SATA 2.0

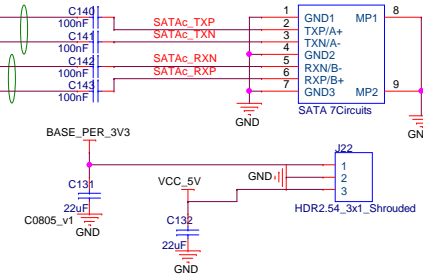
#### LAYOUT NOTE:

SATA Differential Pair, Follow SATA routing guidelines. Differential Impedance: 85 ohms Length match +/-5mil

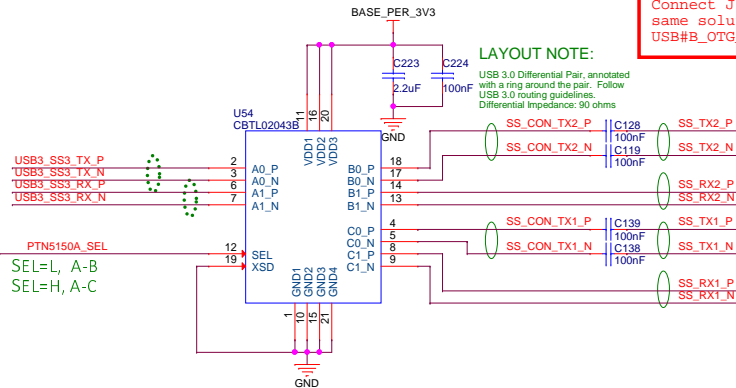
SATA\_TXP  
SATA\_TXN  
SATA\_RXN  
SATA\_RXP

#### LAYOUT NOTE:

Layout Note  
Place AC caps close to the connector



### USB TYPE C Circuitry

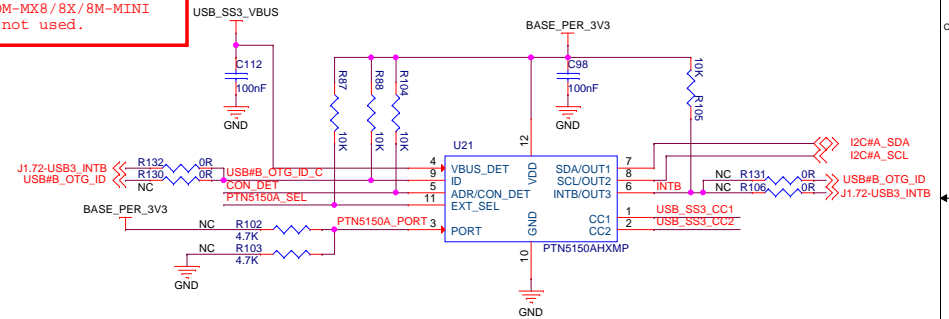


#### LAYOUT NOTE:

USB 3.0 Differential Pair, annotated with a ring around the pair. Follow USB 3.0 routing guidelines. Differential Impedance: 90 ohms

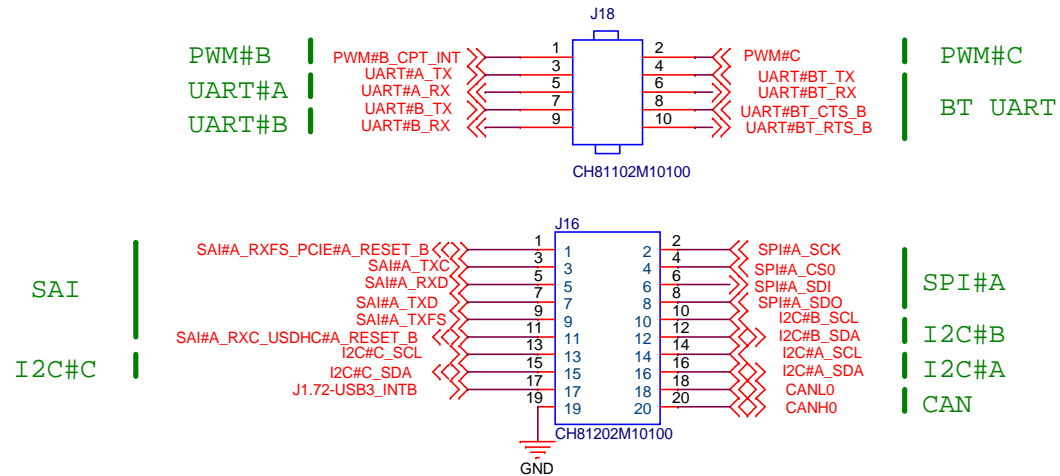
Usage of native USB\_ID for iMX8MP requires patches not included in the formal release, pull up should be to 1.8V.  
For simple OTG function for VAR-SOM-MX8M-PLUS Connect J1.72 GPIO to U22 PTN ID output - same solution applies also for VAR-SOM-MX8/8X/8M-MINI USB#B\_OTG\_ID can be left floating if not used.

### Config Channel Logic Detection & Indication of Plug Orientation

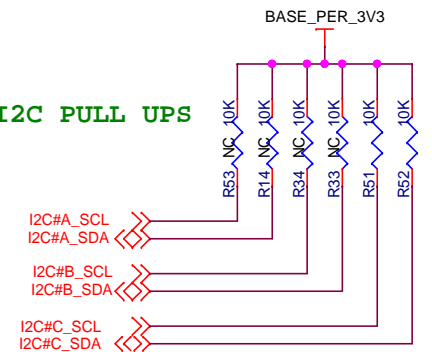


# 14. Headers

Headers arranged for compatible alternate function



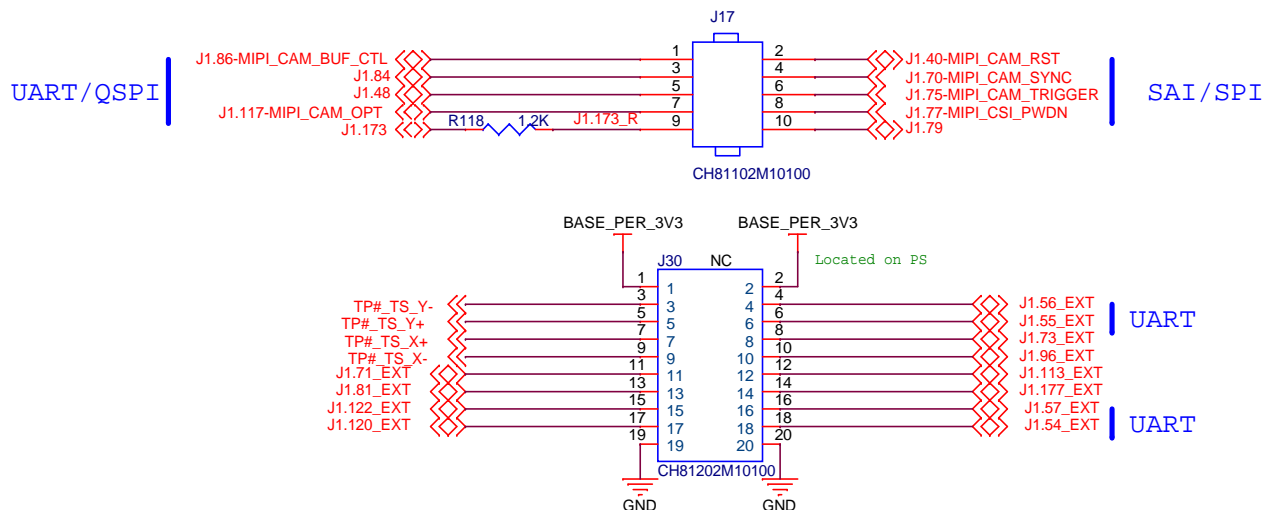
I2C PULL UPS



I2C\_A has internal pulls in Camera buffer

I2C\_B has internal pulls in MX6/MX8/MX8X/MX8MP SOMs.  
For MX8MM/MX8MN/6UL SOMs - external pull ups should be added.

Headers arranged for partial compatible alternate function



**COLD RESET ON WDOG\_B EVENT for MX6/SOLO and 6UL SOMs**

Listed above SOMs require short on headers to get "reboot" to function.  
For all other watch dog looped on SOM

|               |   |           |
|---------------|---|-----------|
| CB_WDOG_B     | >> Symphony Board reset circuitry watch dog input | See J3.17 |
| J1.57_EXT     | << SOM_6UL: PIN57 WDOG1_B                         | See J3.11 |
| PWM#B_CPT_INT | << MX6/SOLO: PIN68 WDOG1_B                        | See J18.1 |

**USB#A Host VBUS power control**

In order to control the USB#A HOST VBUS power a short is required:  
Symphony Board U22

|                      |                                     |           |
|----------------------|-------------------------------------|-----------|
| CB-USB#A_HOST_PWR    | >> Symphony Board U22 control input | See J3.12 |
| J1.82-USB#A_HOST_PWR | >>                                  | See J3.18 |

For complete header alternate function refer to "VAR-SOMs\_Compatibility\_and\_Pinout.XLS" located at:  
[ftp://ftp.variscite.com/SOM\\_Compatibility](ftp://ftp.variscite.com/SOM_Compatibility)

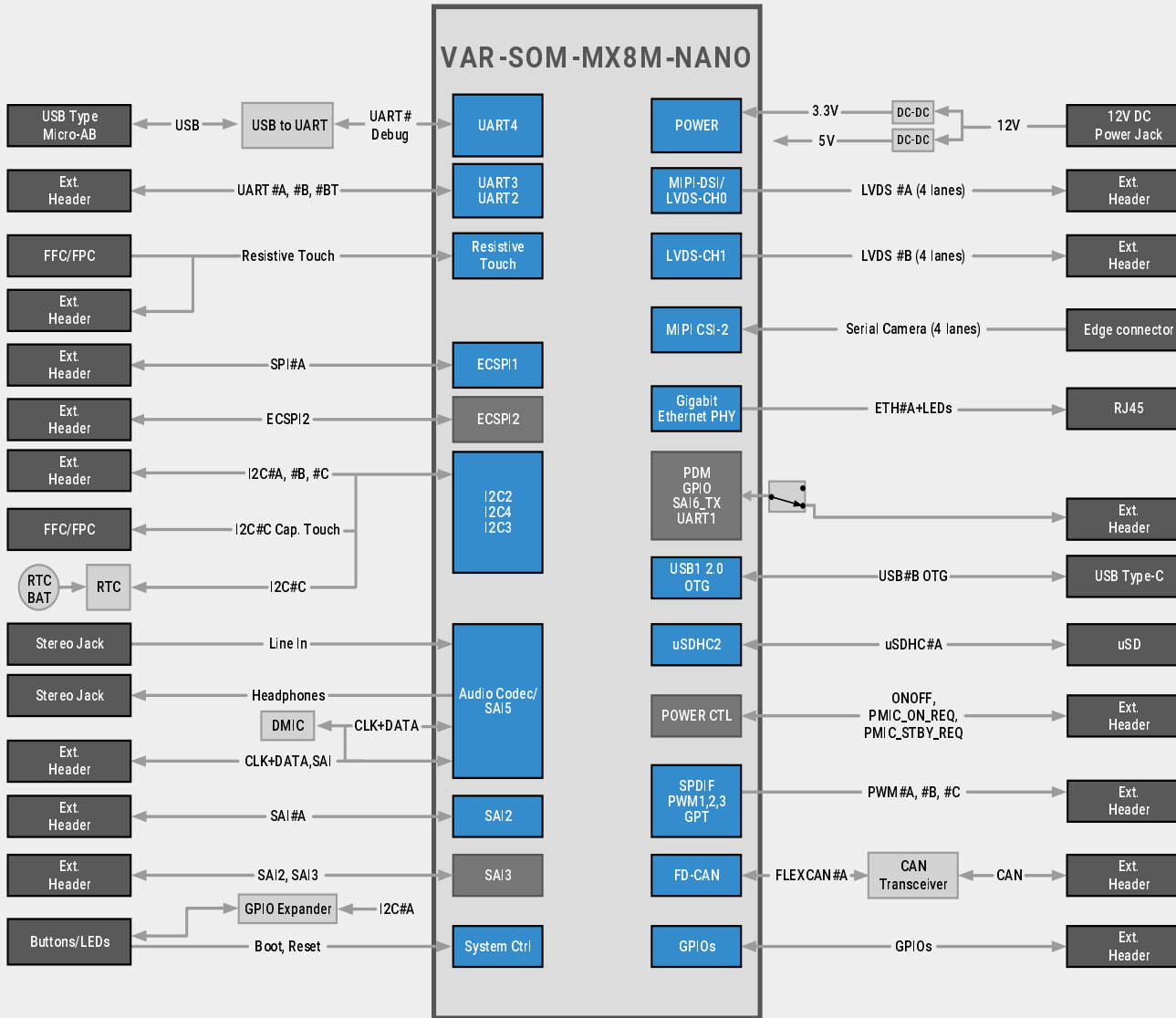


|                                       |                                   |                                |                  |
|---------------------------------------|-----------------------------------|--------------------------------|------------------|
| Title<br>14. Headers                  |                                   |                                |                  |
| Size<br>A4                            | Document Number<br>Symphony-Board | Project<br>Symphony-Board      | Rev<br>1.6C R1.2 |
| Designer:<br>Monday, January 30, 2023 |                                   | Approved By:<br>Sheet 12 of 24 |                  |

## 02. Block Diagram VAR-SOM-MX8M-NANO

### Symphony-Board

Doc rev 1.1



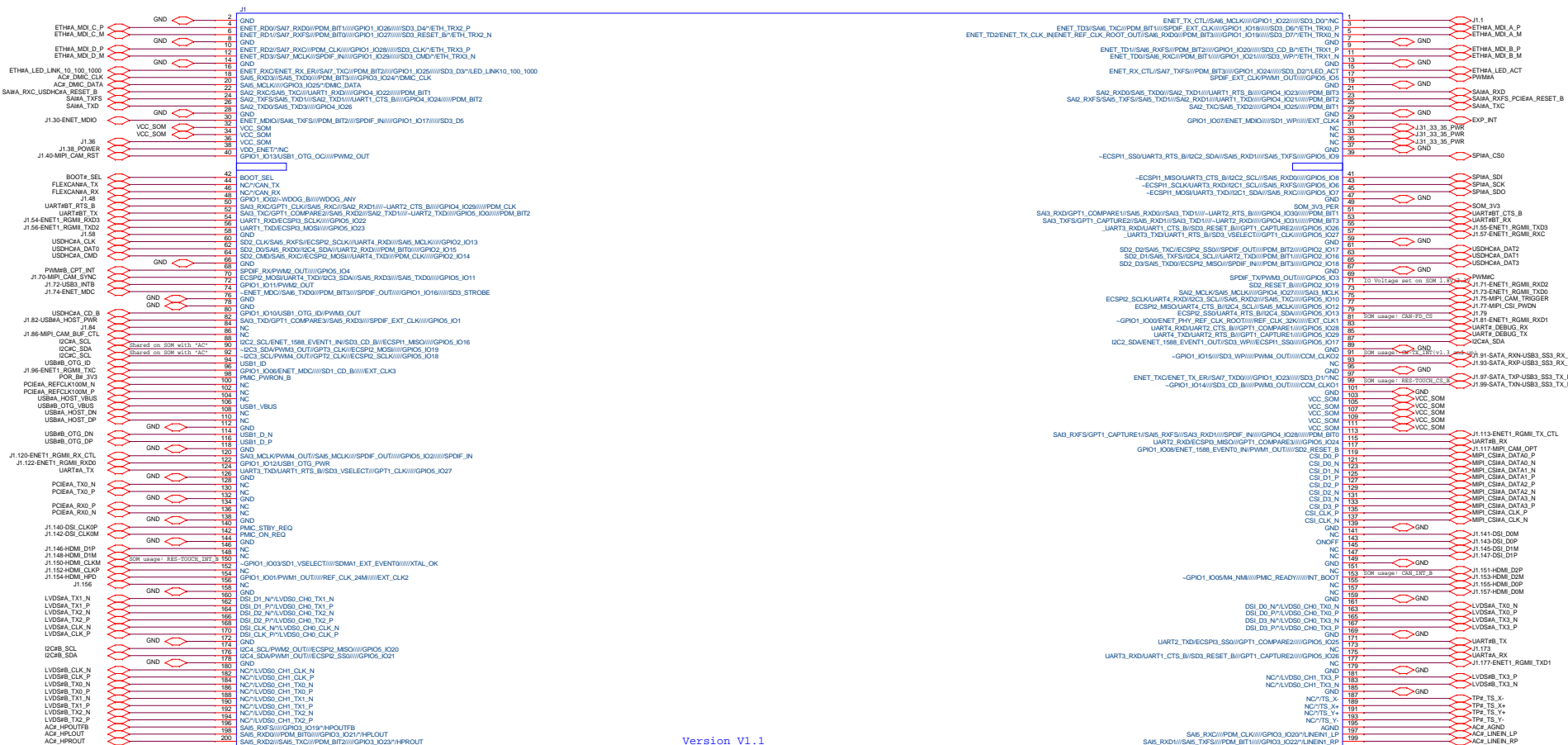
Pin2pin with additional VAR-SOM products.  
Please check pin-list document for details

Not Compatible



|  |                                   |                           |                    |
|--|-----------------------------------|---------------------------|--------------------|
| Title<br>02. Block Diagram VAR-SOM-MX8M-MINI |                                   |                           |                    |
| Size<br>A3                                   | Document Number<br>Symphony-Board | Project<br>Symphony-Board | Rev<br>1.6C, R1.23 |
| Designer<br>Aviad H.                         |                                   | Approved By:              |                    |
| Date<br>Monday, January 30, 2023             |                                   | Sheet<br>19 of 24         |                    |

#### 04. VAR-SOM-MX8M-NANO Connector



### PIN NAMING MNEMONICS:

- "/" - Prefix number of "/" denotes alternate function number; none is ALT0=PAD name
- "/\*" - Prefix denotes pin connected to a configurable module on SOM;  
E.g. with "EC" pin ENET\_TD3////GPIO1\_I018/\*ETH\_TRX0\_P source is Ethernet PHY
- "~" - Prefix points to an alternate function optionally used or shared on SOM;  
Verify with SOM datasheet before using this pin;

Version V1.1

SETUP NOTES FOR VAR-SOM-MX8M-MINI:

EXP\_ENET\_SEL - Set to Header  
Pin 71, 80 IO levels running from NVCC\_SD2 set on SOM:

