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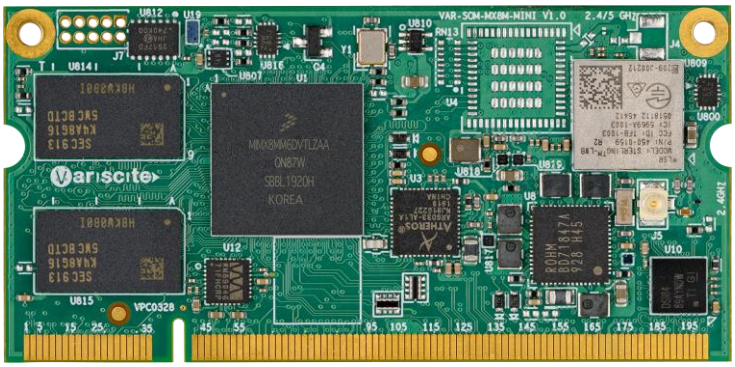
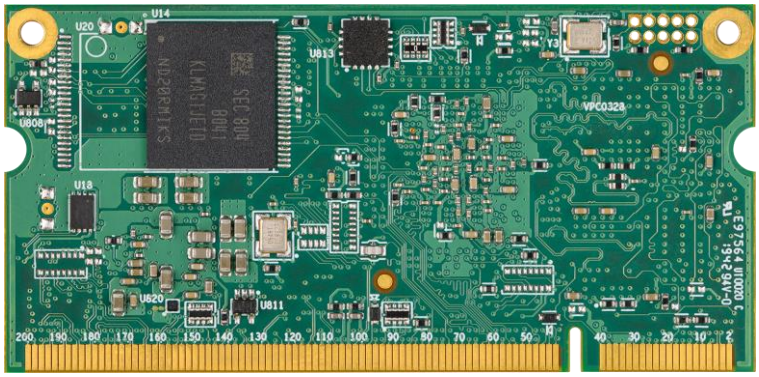
VAR-SOM-MX8M-MINI V1.x Datasheet

NXP i.MX 8M Mini™ - based System-on-Module





VARISCITE LTD.

VAR-SOM-MX8M-MINI Datasheet

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1. Document Revision History

Revision	Date	Notes
1.00	Oct 16, 2019	Preliminary Release
1.01	Jan14, 2020	Official Release Updated pinout pins function/usage for pins: 40 48 72 80 94 97 98 135 137 153
1.02	Jan 20, 2020	Update boot config pins drive from SOM_3V3_PER
1.03	Feb 05, 2020	Updated SOM power requirements Table: 55 see Important Note Updated power consumption Table: 56 updated
1.04	Apr 30, 2020	Add power up timing diagram – see section 8.23.3.1 Add SOM_3V3_PER loading requirement note – see “Table 52: Power Pins “ Added Audio Codec note about RC network – see 8.10.1 Update pins 83&85 for usage of UART4 as Symphony Base board debug UART (old pins 54&56)
1.05	Jun 14, 2020	Updated Table 1 eMMC ordering notation
1.06	Jul 26, 2020	Update power consumption Table 56.
1.07	Mar 18, 2021	Updated Table 1 – delete temperature figures CAN-FD changes for SOM version V1.3 and onward: • CAN-FD controller manufacturer part number updated toMCP2518 and internal connection of RX_INT to an unused IO • Update Block Diagram for CAN-FD RX_INT • Added section 8.16.1 • Added comments for pin 91 use with CAN configuration
1.08	Apr 28, 2021	Updated Reliability data section 10
1.09	Jun 1, 2021	Updated Table 23 – SAI_MCLK direction
1.10	Nov 04, 2021	Updated Block Diagram Added EEPROM section 5.10
1.11	Dec 27, 2021	Added Section 5.1.21 – Degradation of internal IO pullup/pulldown current capability
1.12	Feb 06, 2022	Update the Table in section 6
1.13	Feb 17, 2022	Added Ethernet PHY ADIN1300 – Updated sections 4.3, 5.6, 7.3, 8.5, 9.4 Updated Note for pin 30 Updated section 5.3
1.14	Mar 13, 2022	Corrected ADIN1300 pin numbering Tables 3,11
1.15	May 1, 2022	Updated sections: 4.2, 5.4, 8.6
1.16	Jun 30, 2022	Corrected note section 8.23.3 Corrected standoffs P/N section 11.2
1.17	Dec 26, 2022	Updated section 9.2 USB_VBUS following NXP’s i.MX8M-MINI datasheet update Rev. 2
1.18	Feb 26, 2023	Updated section 10 Updated the eMMC on sections- 4.2, 5.2, 6

2. Table of Contents

3. List of Tables

4. Overview

4.1. General Information

The VAR-SOM-MX8M-MINI offers latest video and audio experience combining state-of-the-art media-specific features with high-performance processing while optimized for lowest power consumption. It perfectly fits various embedded products, the growing market of connected and portable devices and segment for connected streaming audio/video devices, scanning/imaging devices and various devices requiring high-performance, low-power processors.
The product is based on the NXP i.MX 8M MINI family of multi-purpose processors, featuring a quad Arm® Cortex®-A53 core up to 1.8GHz with a general-purpose Cortex®-M4 400 MHz core processor for low-power processing.

This heterogeneous multicore processing architecture enables the device to run an open operating system like Linux on the Cortex-A53 core and an RTOS like FreeRTOS™ on the Cortex-M4 core for time and security critical tasks.

The VAR-SOM-MX8M-MINI MINI provides an ideal building block for simple integration with a wide range of products in target markets requiring high-performance processing with low power consumption, compact size and a very cost-effective solution.

Supporting products:

- Symphony-Board – evaluation board
  - ✓ Carrier Board, compatible with VAR-SOM-MX8X, VAR-SOM-MX8
  - ✓ Schematics
- VAR-DVK-VS8M-MINI full development kit, including:
  - ✓ Symphony-Board
  - ✓ VAR-SOM-MX8M-MINI
  - ✓ Display and touch
  - ✓ Accessories and cables
- O.S support
  - ✓ Linux BSP
  - ✓ Android

Contact Variscite support services for further information: support@variscite.com.

4.2. Feature Summary

- NXP i.MX 8M Mini series SOC
  - i.MX 8M Mini family ARM® Cortex™-A53 Core up to 1.8GHz
  - 400MHz ARM® Cortex™-M4
  - Up to 4GB DDR4 RAM
  - 8-bit up to 128GB eMMC or up to 512MB NAND flash boot and storage
- Display Support
  - Dual channel LVDS display interface
  - MIPI DSI
- Networking
  - 10/100/1000 Mbit/s Ethernet Interface
  - Certified dual band Wi-Fi 802.11 ac/a/b/g/n or single band 802.11 b/g/n Bluetooth: 5.2/BLE
  - CAN-FD
- Camera
  - MIPI-CSI – CMOS Serial camera Interface 4 lanes
- Audio
  - Analog Stereo line in
  - Analog headphones out
  - Digital microphone
  - 6x Digital audio (SAI, SPDIF, PDM)
- USB
  - 2 x USB 2.0 OTG
- Other Interfaces
  - SDIO/MMC
  - PCIe v2.0
  - Serial interfaces (ECSPI, I2C, UART, JTAG)
  - GPIOs
  - Resistive Touch
- Single power supply: 3.3V
- Dimensions (W X L X H): 67.6 x 33.0 x 3.9 [mm]
- Industrial temperature range: -40 to 85ºC

4.3. Block Diagram

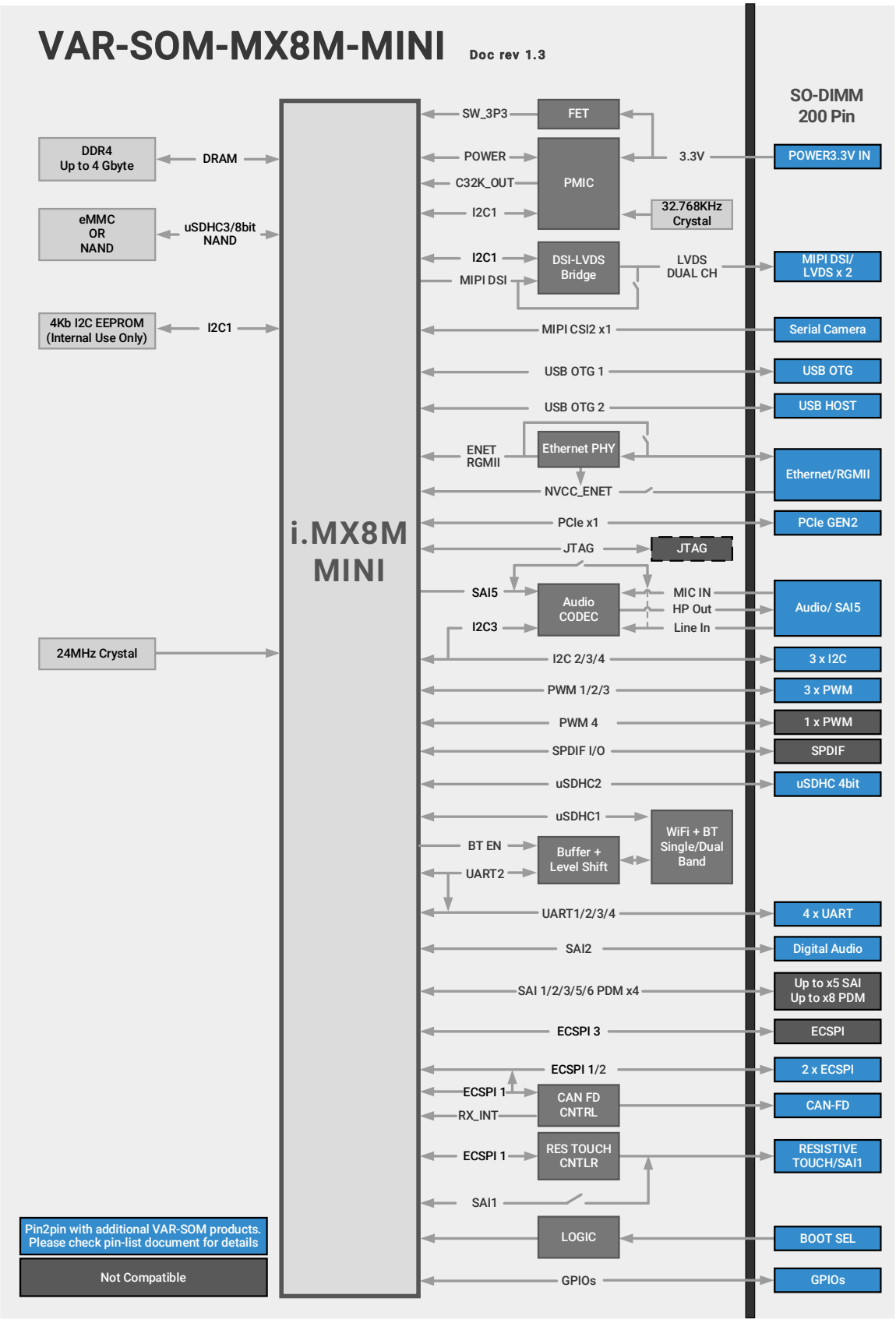


Figure 1 : VAR-SOM-MX8M-MINI Block Diagram

5. Main Hardware Components

This section summarizes the main hardware building blocks of the VAR-SOM-MX8M-MINI.

5.1. NXP i.MX 8M Mini

5.1.1. Overview

The i.MX 8M MINI is a family of products focused on delivering an excellent video and audio experience, combining media-specific features with high-performance processing optimized for low-power consumption.
The i.MX 8M MINI Media Applications Processor is built to achieve both high performance and low power consumption and rely on a powerful fully coherent core complex based on a quad Cortex-A53 cluster with video and graphics accelerators.
The i.MX 8M Family provides additional computing resources and peripherals:

- Advanced security modules for secure boot, cipher acceleration and DRM support
- General purpose Cortex-M4 processor for low power processing
- A wide range of audio interfaces including I2S, AC97, TDM and S/PDIF
- Large set of peripherals that are commonly used in consumer/industrial markets including USB 2.0, PCIe and Ethernet

5.1.2. i.MX8M-MINI Block Diagram

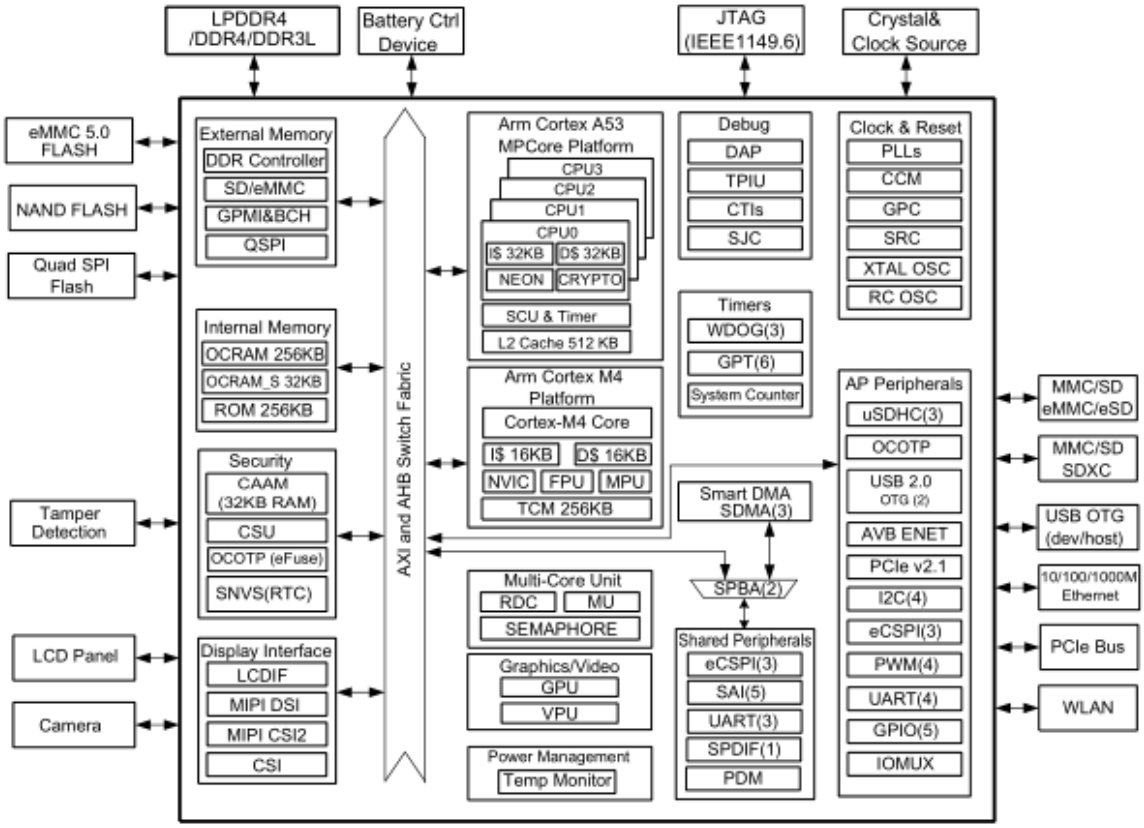


Figure 2 : i.MX 8M Mini Block Diagram

5.1.3. ARM Cortex-A53 MPCore™ Platform

- The i.MX 8M Family Applications Processors are based on the Arm Cortex-A53 MPCore™ Platform, which has the following features:
    - Quad symmetric Cortex-A53 processors, including:
        - 32 KB L1 Instruction Cache
        - 32 KB L1 Data Cache
        - Media Processing Engine (MPE) with NEON technology supporting the Advanced Single Instruction Multiple Data architecture
    - Floating Point Unit (FPU) with support of the VFPv4-D16 architecture
    - Support of 64-bit Armv8-A architecture
    - 512 KB unified L2 cache
    - Target frequency of 2GHz

5.1.4. Arm Cortex-M4 Platform

Cortex-M4 Core Platform include the following:

• Low power microcontroller available for customer application:
    - Low power standby mode
    - IoT features including Weave
    - Manage IR or wireless remote

• Arm Cortex M4 CPU Processor, including:
    - 16 KB L1 Instruction Cache
    - 16 KB L1 Data Cache
    - 256 KB TCM
    - Target frequency of 400MHz

5.1.5. System Bus and Interconnect

System bus and interconnect include the following:

- Network interconnect (NoC) AXI arbiter
- Quality of service controller (QoSC) to configure priorities and limits of AXI transactions
- Performance monitor (PERFMON) to monitor AXI bus activity
- Debug monitor (DBGMON) to record AXI transactions preceding a system reset

5.1.6. Clocking and Resets

Clocking and resets include:

- Clock control module (CCM) provides centralized clock generation and control
    - Simplified clock tree structure
    - Unified clock programming model for each clock root
    - Multicore awareness for resource domains
- System reset controller (SRC) provides reset generation and distribution

5.1.7. Interrupts and DMA

Interrupts and DMA include:

- 128 shared peripheral interrupts routed to Cortex-A53 Global Interrupt Controller (GIC) and Cortex-M4 nested vector interrupt controller (NVIC) for flexible interrupt handling
- Three Smart direct memory access (SDMA) engines. Although these three engines are identical to each other, they are integrated into the processor to serve different peripherals.
    - SDMA-1 is a general-purpose DMA engine which can be used by low speed peripherals including UART, SPI and also others peripherals.
    - SDMA-2 and SMDA-3 is used for audio interface, including SAI-1/2/3/5/6, SPDIF and PDM audio input.

5.1.8. On-Chip Memory

The on-chip memory system consists of the following:

- Boot ROM (256KB)
- On-chip RAM (256KB + 32KB)

5.1.9. External Memory Interface

The external memory interfaces supported on this chip include:

- 16/32-bit DRAM Interface:
    - DDR4-2400
- 8-bit NAND FLASH, including support for Raw MLC/SLC devices, BCH ECC up to 62-bit, and ONFi3.2 compliance (clock rates up to 100 MHz and data rates up to 200 MB/sec)
- eMMC 5.0 FLASH (2 interfaces)
- SPI NOR FLASH (3 interfaces)
- FlexSPI FLASH with support for XIP (for M4 in low-power mode) and parallel read mode of two identical FLASH devices

5.1.10. Timers

The timers on this chip include:

- One local generic timer integrated into each Cortex-A53 CPU
- Global system counter with timer bus interface to Cortex-A53 MPCore generic timers
- One local system timer (SysTick) integrated into the Cortex-M4 CPU
- Six general purpose timer (GPT) modules
- Three watchdog timer (WDOG) modules
- Four pulse width modulation (PWM) modules

5.1.11. Graphics Processing Unit (GPU)

The chip incorporates the following Graphics Processing Unit (GPU) features:

- 2D/3D acceleration
- Target frequency of 800 MHz
- Support OpenGL ES 1.1, 2.0, OpenVG 1.1
- TrustZone support using a local MMU to manage secure regions
- Support multi-source composition
- Support one-pass filter
- Support tile format

5.1.12. Video Processing Unit (VPU)

The chip incorporates the following Video Processing Unit (VPU) features:

- 1080p60 VP9 Profile 0, 2 (10 bit) Decoder (Hantro G2)
- 1080p60 HEVC/H.265 Decoder (Hantro G2)
- 1080p60 AVC/H.264 Baseline, Main, High Decoder (Hantro G1)
- 1080p60 VP8 Decoder (Hantro G1)
- 1080p60 AVC/H.264 Encoder (Hantro H1)
- 1080p60 VP8 Encoder (Hantro H1)
- TrustZone support

5.1.13. Display/Camera Interfaces

The chip has the following display/camera support:

- LCDIF Display Controller:
  - Supports up to 2 layers of overlay
  - Support up to 1080p60 display through MIPI DSI
- MIPI Interface:
  - 4-lane MIPI CSI interface
  - 4-lane MIPI DSI interface
- CSI Interface:
  - CSI is a simple camera interface which is used to capture the MIPI CSI input and save the pixels into memory

5.1.14. Audio

Audio include the following:

- S/PDIF Input and Output, including a new Raw Capture input mode
- Five external SAI (synchronous audio interface) modules supporting I2S, AC97, TDM, codec/DSP and DSD interfaces, including one SAI with 8 TX and 8 RX lanes, one SAI with 4 TX and 4 RX lanes, two SAI with 2 TX and 2 RX lanes, and one SAI with 1 TX and 1 RX lanes. Supports over 20 channels of audio subject to I/O limitations.
- Four channels of PDM (Digital Microphone Interfaces)

5.1.15. General Connectivity Interfaces

The chip contains a rich set of general connectivity interfaces, including:

- One PCI Express (PCIe):
  - Single lane supporting PCIe Gen 2
  - Dual mode operation to function as root complex or endpoint
  - Integrated PHY interface
  - Supports L1 low power substate
- Two USB 2.0 OTG controllers with integrated PHY interface
  - Spread spectrum clock support
- Three Ultra Secure Digital Host Controller (uSDHC) interfaces
  - MMC 5.0 compliance with HS400 DDR signaling to support up to 400 MB/sec
  - SD/SDIO 3.01 compliance with 200 MHZ SDR signaling to support up to 100 MB/sec
  - Support for SDXC (extended capacity)
- One Gigabit Ethernet controller with support for EEE, Ethernet AVB and IEEE1588
- Four universal asynchronous receiver/transmitter (UART) modules
- Four I2C modules
- Three SPI modules

5.1.16. Security

Security functions are enabled and accelerated by the following hardware:

- RDC – Resource Domain Controller:
  - Supports 4 domains and up to 8 regions
- Arm TrustZone including the TZ architecture:
  - ARM Cortex-A53 MPCore TrustZone support
- On-chip RAM (OCRAM) secure region protection using OCRAM controller
- High Assurance Boot (HAB)
- Cryptographic Acceleration and Assurance Module (CAAM)
  - Support Widevine and PlayReady content protection
  - Public Key Cryptography (PKHA) with RSA and Elliptic Curve (ECC)
  - algorithms
  - Real-time integrity checker (RTIC)
  - DRM support for RSA, AES, 3DES, DES
  - Side channel attack resistance
  - True random number generation (RNG)
  - Manufacturing protection support
- Secure Non-Volatile Storage (SNVS), including
  - Secure Real Time Clock (RTC)
- Secure JTAG Controller (SJC)

5.1.17. Multicore Support

Multicore support contains:

- Resource domain controller (RDC) to support isolation and safe sharing of system resources
- Messaging unit (MU)
- Hardware Semaphore (SEMA42)
- Shared bus topology

5.1.18. GPIO and Pin Multiplexing

- General-purpose input/output (GPIO) modules with interrupt capability
- Input/output multiplexing controller (IOMUXC) to provide centralized pad control

5.1.19. Power Management

The power management unit consists of:

- Temperature sensor with programmable trip points
- Flexible power domain partitioning with internal power switches to support efficient power management

5.1.20. System Debug

The system debug features are:

- ARM CoreSight debug and trace architecture
- Trace Port Interface Unit (TPIU) to support off-chip real-time trace
- Embedded Trace FIFO (ETF) with 4 KB internal storage to provide trace buffering
- Unified trace capability for Quad Cortex-A53 and Cortex-M4 CPUs
- Cross-Triggering Interface (CTI)
- Support for 5-pin (JTAG) debug interfaces

5.1.21. Degradation of internal IO pullup/pulldown current capability

According to latest NXP Errata ERR050080 there is a degradation of the internal IO pullup/pulldown capability when the IO pads are continuously driven in the opposite logic level.

For example, when internal pullup is enabled with external logic driving the pin low, and a 3.3V operating condition which limits the pads pullup/pulldown ability.
All IO pin groups are impacted except for XTAL, DDR, PCI, USB, and MIPI PHY IO's.

The suggested workaround is to use external resistors for the pullup/pulldown and disable the internal pullup/pulldown via software on pins that operate at 3.3V and the circuit requires pullup or pulldown

5.2. Memory

5.2.1. RAM

The VAR-SOM-MX8M-MINI is available with up to 4GB GB of DDR4 memory capable of running up to 2400MTS.

5.2.2. Non-volatile Storage Memory

The VAR-SOM-MX8M-MINI is available with a non-volatile storage memory with optional densities. It is used for Flash Disk purposes, O.S. run-time-image, Boot-loader and application/user data storage.
The VAR-SOM-MX8M-MINI can arrive with up to 128GB MLC eMMC or NAND with density up to 512MB.

5.3. Audio (WM8904)

The WM8904 is a high performance ultra-low power stereo CODEC optimized for portable audio applications.
The device features stereo ground-referenced headphone amplifiers using the Wolfson 'Class-W' amplifier techniques. It incorporates an innovative dual-mode charge pump architecture - to optimize efficiency and power consumption during playback.
The ground-referenced headphone output eliminates AC coupling capacitors, and both outputs include common mode feedback paths to reject ground noise. Control sequences for audio path setup can be pre-loaded and executed by an integrated control write sequencer to reduce software driver development and minimize pops and clicks via SilentSwitch™ technology. The input impedance is constant with PGA gain setting. A stereo digital microphone interface is provided, with a choice of two inputs. A dynamic range controller provides compression and level control to support a wide range of portable recording applications. Anti-clip and quick release features offer good performance in the presence of loud impulsive noises. ReTuneTM Mobile 5-band parametric equalizer with fully programmable coefficients is integrated for optimization of speaker characteristics. Programmable dynamic range control is also available for maximizing loudness, protecting speakers from clipping and preventing premature shutdown due to battery droop. Common audio sampling frequencies are supported from a wide range of external clocks, either directly or generated via the FLL.

Features:

- 3.0mW quiescent power consumption for DAC to headphone playback
- DAC SNR 96dB typical, THD -86dB typical
- ADC SNR 91dB typical, THD -80dB typical
- 2.4mW quiescent power consumption for analogue bypass playback
- Control write sequencer for pop minimized start-up and shutdown
- Single register writes for default start-up sequence
- Integrated FLL provides all necessary clocks - Self-clocking modes allow processor to sleep - All standard sample rates from 8kHz to 96kHz
- Stereo digital microphone input
- 2 single ended inputs per stereo channel
- Digital Dynamic Range Controller (compressor / limiter)
- Digital sidetone mixing
- Ground-referenced headphone driver

5.4. Wi-Fi + BT

VAR-SOM-MX8M-MINI module can be configured either for Dual band or Single Band Wi-Fi® and Bluetooth® add on modules. Both realize the necessary PHY/MAC layers to support WLAN applications in conjunction with a host processor over a SDIO interface.
The modules also provide a Bluetooth/BLE platform through the HCI transport layer. Both WLAN and Bluetooth share the same antenna port.

VAR-SOM-MX8M-MINI Wi-Fi and BT Key Features:

- IEEE 802.11 ac/a/b/g/n (Dual Band Option)
- IEEE 802.11 b/g/n (Single Band Option)
- Bluetooth 2.1+EDR, and BLE 5.2
- U.F.L connector for external antenna
- Latest Linux and Android drivers supported directly by LSR and Cypress
- Wi-Fi/BT module Broad certifications with multiple antennas: FCC (USA), IC (Canada), ETSI (Europe), Giteki (Japan), and RCM (AU/NZ)
- Industrial operating Temperature Range: -40 to +85

5.4.1. VAR-SOM-MX8M-MINI Dual Band Option

The VAR-SOM-MX8M-MINI contains LSR's certified high-performance Sterling-LWB5™ Dual band 2.4/5 GHz Wi-Fi® and Bluetooth® Smart Ready Multi-Standard Module based upon the Cypress (formerly Broadcom) CYW43353 chipset supporting 802.11 ac/a/b/g/n, BT 2.1+EDR, and BLE 5.2 wireless connectivity.

5.4.2. VAR-SOM-MX8M-MINI Single Band Option

The VAR-SOM-MX8M-MINI contains LSR's certified high-performance Sterling-LWB™ 2.4 GHz Wi-Fi® and Bluetooth® Smart Ready Multi-Standard Module based upon the Cypress (formerly Broadcom) CYW4343W chipset supporting IEEE 802.11 b/g/n,
BT 2.1+EDR, and BLE 4.2 wireless connectivity.

5.5. PMIC

The VAR-SOM-MX8M-MINI features ROHM PN:BD71847AMWV as a Power Management Integrated circuit (PMIC) designed specifically for use with NXP's i.MX8M-MINI series of application processors. The PMIC regulates all power rails required on SOM from a single power supply with 3.3V.

The PMIC is fully programmable via the I2C interface and associated register map. Additional communication is provided by direct logic interfacing including interrupt, watchdog and reset.

5.6. 10/100/1000 Mbps Ethernet Transceiver

The VAR-SOM-MX8M-MINI can be ordered with an Integrated Ethernet Transceiver, Qualcomm Atheros AR8033 or Analog Devices ADIN1300.
Please contact sales@variscite.com for inquiries about P/N assembled on your SOM.

5.6.1. Qualcomm Atheros AR8033 Ethernet Transceiver

Key features include:

- 10BASE-Te/100BASE-TX/1000BASE-T IEEE 802.3 compliant
- 1000BASE-T PCS and auto-negotiation with next page support
- Green ETHOS power saving modes with internal automatic DSP power saving scheme
- IEEE 802.3az EEE
- Fully integrated digital adaptive equalizers, echo cancellers, and Near End Crosstalk (NEXT) cancellers
- Robust Cable Discharge Event (CDE) protection of ±6 kV
- Robust operation over up to 140 meters of CAT5 cable
- Automatic Channel Swap (ACS)
- Automatic MDI/MDIX crossover
- Automatic polarity correction ν IEEE 802.3u compliant auto-negotiation
- Jumbo frame supports up to 10 KB (full-duplex)
- Integrated termination circuitry at the line side

5.6.2. Analog Devices ADIN1300 Ethernet Transceiver

Key features include:

- 10BASE-Te/100BASE-TX/1000BASE-T IEEE® 802.3™ compliant MII, RMII, and RGMII MAC interfaces
- EEE in accordance with IEEE 802.3az
- Start of packet detection for IEEE 1588 time stamp support
- Enhanced link detection
- Configurable LED
- Integrated power supply monitoring and POR
- MII management interface (MDIO) compatible with the IEEE 802.3 Standard Clause 22 and Clause 45 management frame structures.

- Supports cable lengths up to 150 meters at Gigabit speeds and 180 meters when operating at 100 Mbps or 10 Mbps.
- Automatic MDI/MDIX crossover
- Autonegotiation capability in accordance with IEE 802.3 Clause 28
- Supports a number of power-down modes: hardware, software, and energy detect power-down, and EEE LPI mode
- On-chip cable diagnostics capabilities
- Transmit drivers are voltage mode with on-chip terminations

5.7. MIPI-DSI to Dual Channel LVDS Bridge (SN65DSI84)

The VAR-SOM-MX8M-MINI features TI SN65DIS84 MIPI-DSI Bridge to FLATLINK LVDS display.

The SN65DSI84 DSI to FlatLink™ bridge features a single-channel MIPI® D-PHY receiver front-end configuration with 4 lanes per channel operating at 1 Gbps per lane. The bridge decodes MIPI® DSI 18bpp RGB666 and 24 bpp RGB888 packets and converts the formatted video data stream to a FlatLink™ compatible LVDS output operating at pixel clocks operating from 25 MHz to 154 MHz, offering a Dual-Link LVDS, Single-Link LVDS interface with four data lanes per link.
The SN65DSI84 is well suited for WUXGA 1920 x1200 at 60 frames per second, with up to 24 bits-per-pixel. Partial line buffering is implemented to accommodate the data stream mismatch between the DSI and LVDS interfaces.
Designed with industry compliant interface technology, the SN65DSI84 is compatible with a wide range of micro-processors and is designed with a range of power management features including low running swing LVDS outputs, and the MIPI® defined ultra-low power state (ULPS) support.

5.8. CAN-FD Controller (MCP2518FD)

The VAR-SOM-MX8M-MINI features Microchip MCP2518FD CAN FD controller.

Key features include:

- SPI Interface with modes 0, 0 and 1, 1
- Arbitration Bit Rate up to 1 Mbps
- Data Bit Rate up to 8 Mbps
- CAN FD Controller modes
  - Mixed CAN 2.0B and CAN FD mode
  - CAN 2.0B Mode
- Conforms to ISO 11898-1:2015
- Discrete IO interrupt pin
- Up to 20MHz SPI clock speed

5.9. Touch Panel Controller (TSC2046I)

The VAR-SOM-MX8M-MINI features BB TSC2046 a 4-wire touch screen controller.

Key features include:

- Reference can also be powered down when not used to conserve power.
- Low power consumption
- SPI Interface
- High-speed (up to 125kHz sample rate)
- On-chip drivers make the TSC2046 an ideal choice for battery-operated systems such as personal digital assistants (PDAs) with resistive touch screens, pagers, cellular phones, and other portable equipment.
- Specified over the –40°C to +85°C temperature range.

5.10. EEPROM

The SOM uses 4Kbit serial EEPROM to store memory calibration and manufacturing parameters.
This EEPROM is connected to I2C1 bus and intended only for holding the above information.
The SOM may not boot if the contents of EEPROM device are corrupted.

6. VAR-SOM-MX8M-MINI Hardware Configuration

VAR-SOM-MX8M-MINI hardware interfaces, explained on sections 5.3, 5.4, 5.6.2 and 5.6, configured using the orderable part number of the module.

For every hardware configuration option, the SOM pinout will be affected, see section 7.3 for complete list.

Table 1 details part of the hardware configuration orderable options.

Table 1: Partial Hardware Configuration Options

OPTION	DESCRIPTION
EC	**E**thernet **C**ontroller PHY assembled on SOM
AC	**A**udio **C**odec assembled on SOM
WBD **WB**	**W**i-Fi **B**luetooth (BT/BLE) **D**ual band - combo assembled on SOM **W**i-Fi **B**luetooth (BT/BLE) Single band - combo assembled on SOM
LD	**L**VDS **D**isplay bridge assembled on SOM
0xG	**NAND** Configuration size – **Not released Yet!**
xG	**eMMC** Configuration size: 8G/16G/32G/64G/128G (8/16/32/64/128 GB)
TP	**T**ouch **P**anel controller assembled on SOM
CN	**CAN**-FD controller assembled on SOM
CT **ET** **IT**	Temperature grade: **CT** - Commercial Temperature E**T** - Extended Temperature **IT** – Industrial Temperature

NOTE

Other orderable options are available and are not part of this datasheet.
Please *Contact Information* for complete list of configuration options.

7. External Connectors

7.1. Board to Board Connector

- The VAR-SOM-MX8M-MINI exposes one 200-pin SO-DIMM edge connector.
- The recommended mating connectors for baseboard interfacing are:
    1. Concraft - 0701A0BE52E
    2. Tyco Electronics -1565917-4

7.2. Wi-Fi & BT Connector

- Modules with Wi-Fi ***"WBD" or "WB" Configuration*** **-** a combined Wi-Fi + BT antenna connector is assembled
- Connector type: **U.FL JACK connector**
- Cable and antenna shall have a 50 Ohm characteristic impedance

7.3. VAR-SOM-MX8M-MINI Connector Pin-out

Tables under this section lists the SOM connectors pinout with each pin listed for all the available ball names related to the assembly hardware configuration options.

Table 2: PIN-OUT Tables Mnemonics

Column Heading		Meaning
PIN#		Pin number on a connector
ASSY		Can be any of the **options listed in Table 1**. **"NO"** - will be added to above option - means the option is not part of the SOM part number. **Blank** - pin listed have no hardware configuration option **NC** - Pin is Not Connected
BALL NAME		Name of the ball for the specific ASSY option
GPIO	**GPIOx_y**	SOC pin GPIO Alternate function number including: **x- GPIO bank** **y-Bit number in the bank**
NOTES		This column displays any special note related to the specific pin with the specific ASSY The notes will repeat also in the function tables.
BALL		Source device and it's pin number.
	XX.YY	XX: Source Chip can be: SOC.yy – pins connected to the iMX8M SoC AR8033.yy/ ADIN1300.yy – pins connected the Ethernet Controller (***"EC" Configuration***) WM8904.yy - pins connected the Audio Codec (***"AC" Configuration***) SN65DSI84.yy - pins connected the LVDS Display bridge (***"LD" Configuration***) MCP2518.yy - pins connected the CAN-FD controller (**"CN" Configuration**) TSC2046.yy - pins connected the Touch Panel controller (**"TP" Configuration**) YY : Pin/Ball number of source chip.

NOTE

A. Some pins may appear in several consecutive lines if additional chip function used on SOM; Relates to the VAR-SOM-MX8M-MINI orderable hardware configuration.

B. In case a chip is added due to an orderable configuration the chip function must be used.

7.3.1. VAR-SOM-MX8M-MINI SO-DIMM Pin-out

Table 3: SO-DIMM PIN-OUT

PIN#	ASSY	BALL NAME	GPIO	NOTES	BALL
1	No EC	ENET_TX_CTL	GPIO1_IO22	Powered by VDD_ENET pin; On some SOM modules this pin is GND; If placed in such carrier with no "EC" configuration define PAD as input!	SOC.AF24
1	EC	NC		With "EC" configuration this pin in Not Connected.	NC_EC
2		GND		Digital Ground	GND
3	No EC	ENET_TD3	GPIO1_IO18	Powered by VDD_ENET pin	SOC.AF25
3	EC	ETH_TRX0_P		Signal source is Ethernet PHY.	AR8033.11/ ADIN1300.12
4	No EC	ENET_RD0	GPIO1_IO26	Powered by VDD_ENET pin	SOC.AE27
4	EC	ETH_TRX2_P		Signal source is Ethernet PHY.	AR8033.17/ ADIN1300.16
5	No EC	ENET_TD2	GPIO1_IO19	Powered by VDD_ENET pin	SOC.AG25
5	EC	ETH_TRX0_N		Signal source is Ethernet PHY.	AR8033.12/ ADIN1300.13
6	No EC	ENET_RD1	GPIO1_IO27	Powered by VDD_ENET pin	SOC.AD27
6	EC	ETH_TRX2_N		Signal source is Ethernet PHY.	AR8033.18/ ADIN1300.17
7		GND		Digital Ground	GND
8		GND		Digital Ground	GND
9	No EC	ENET_TD1	GPIO1_IO20	Powered by VDD_ENET pin	SOC.AF26
9	EC	ETH_TRX1_P		Signal source is Ethernet PHY.	AR8033.14/ ADIN1300.14
10	No EC	ENET_RD2	GPIO1_IO28	Powered by VDD_ENET pin	SOC.AD26
10	EC	ETH_TRX3_P		Signal source is Ethernet PHY.	AR8033.20/ ADIN1300.18
11	No EC	ENET_TD0	GPIO1_IO21	Powered by VDD_ENET pin	SOC.AG26
11	EC	ETH_TRX1_N		Signal source is Ethernet PHY.	AR8033.15/ ADIN1300.15
12	No EC	ENET_RD3	GPIO1_IO29	Powered by VDD_ENET pin	SOC.AC26
12	EC	ETH_TRX3_N		Signal source is Ethernet PHY.	AR8033.21/ ADIN1300.19
13		GND		Digital Ground	GND
14		GND		Digital Ground	GND
15	No EC	ENET_RX_CTL	GPIO1_IO24	Powered by VDD_ENET pin	SOC.AF27
15	EC	ETH_LED_ACT		Signal source is Ethernet PHY.	AR8033.23/ ADIN1300.21
16	No EC	ENET_RXC	GPIO1_IO25	Powered by VDD_ENET pin; Includes series EMI filter	SOC.AE26
16	EC	ETH_LED_LINK10_100_1000		Signal source is Ethernet PHY.	AR8033.24_26/ ADIN1300.26 via inverting FET
17		SPDIF_EXT_CLK	GPIO5_IO05		SOC.AF8
18	No AC	SAI5_RXD3	GPIO3_IO24	With “AC” configuration do not alter PINMUX function.	SOC.AC13
18	AC	DMIC_CLK		Signal source is Audio Codec.	WM8904.1
19		GND		Digital Ground	GND

PIN#	ASSY	BALL NAME	GPIO	NOTES	BALL
20	No AC	SAI5_MCLK	GPIO3_IO25	With “AC” configuration do not alter PINMUX function.	SOC.AD15
20	AC	DMIC_DATA		Signal source is Audio Codec.	WM8904.27
21		SAI2_RXD0	GPIO4_IO23		SOC.AC24
22		SAI2_RXC	GPIO4_IO22		SOC.AB22
23		SAI2_RXFS	GPIO4_IO21		SOC.AC19
24		SAI2_TXFS	GPIO4_IO24		SOC.AD23
25		SAI2_TXC	GPIO4_IO25		SOC.AD22
26		SAI2_TXD0	GPIO4_IO26		SOC.AC22
27		GND		Digital Ground	GND
28		GND		Digital Ground	GND
29		GPIO1_IO07	GPIO1_IO07		SOC.AF11
30		ENET_MDIO	GPIO1_IO17	Shared on SOM with "EC"; Includes 1.5K Ohm PU to VDD_ENET; Do not alter pinmux with "EC" configuration	SOC.AB27
31		NC		High power modules VCC_SOM Other GND Current SOM Not connect for compatibility	NC_VCC_SOM_GND
32		VCC_SOM		SOM Power	VCC_SOM
33		NC		High power modules VCC_SOM Other GND Current SOM Not connect for compatibility	NC_VCC_SOM_GND
34		VCC_SOM		SOM Power	VCC_SOM
35		NC		High power modules VCC_SOM Other GND Current SOM Not connect for compatibility	NC_VCC_SOM_GND
36		VCC_SOM		SOM Power	VCC_SOM
37		GND		Digital Ground	GND
38	No EC	VDD_ENET		ENET pins group power IN	SOC.W22
38	EC	NC		With "EC" configuration this pin in Not Connected.	NC_EC
39		ECSPI1_SS0	GPIO5_IO09		SOC.B6
40		GPIO1_IO13	GPIO1_IO13		SOC.AD9
41		ECSPI1_MISO	GPIO5_IO08	Shared internally with "CN" or "TP"	SOC.A7
42		BOOT_SEL		Controls internal OR external boot source; Include 100K pull up to NVCC_SNVS_1V8; Connected via diode for 3.3V compatibility	Int. Boot Logic input
43		ECSPI1_SCLK	GPIO5_IO06	Shared internally with "CN" or "TP"	SOC.D6
44	No CN	NC		Pin not connected with No "CN" configuration!	NC_No_CAN
44	CN	CAN_TX		Signal source is CAN FD controller.	MCP2517.1
45		ECSPI1_MOSI	GPIO5_IO07	Shared internally with "CN" or "TP"	SOC.B7
46	No CN	NC		Pin not connected with No "CN" configuration!	NC_No_CAN
46	CN	CAN_RX		Signal source is CAN FD controller.	MCP2517.2
47		GND		Digital Ground	GND

PIN#	ASSY	BALL NAME	GPIO	NOTES	BALL
48		GPIO1_IO02	GPIO1_IO02	Connected internally to PMIC WDOG_B input; Configured by default DTS to WDOG_B alternate function. PMIC behavior can be programmed to Cold or Warm or no reset.	SOC.AG13
49		SOM_3V3_PER		Power output from SOM; Rises with last power rail; Can be used to control base board power.	SOM_3V3_PER
50		SAI3_RXC	GPIO4_IO29	Used internally with "WBD"; Function can be released if BT Buffer disabled.	SOC.AG7
51		SAI3_RXD	GPIO4_IO30	Used internally with "WBD"; Function can be released if BT Buffer disabled.	SOC.AF7
52		SAI3_TXC	GPIO5_IO00	Used internally with "WBD"; Function can be released if BT Buffer disabled.	SOC.AG6
53		SAI3_TXFS	GPIO4_IO31	Used internally with "WBD"; Function can be released if BT Buffer disabled.	SOC.AC6
54		UART1_RXD	GPIO5_IO22		SOC.E14
55		UART3_RXD	GPIO5_IO26	Appear on pins 55 & 175 for other SOM modules UART compatibility	SOC.E18
56		UART1_TXD	GPIO5_IO23		SOC.F13
57		UART3_TXD	GPIO5_IO27	Appear on pins 57 & 124 for other SOM modules UART compatibility	SOC.D18
58		GND		Digital Ground	GND
59		GND		Digital Ground	GND
60		SD2_CLK	GPIO2_IO13	Bank voltage set on SOM 1.8V/3.3V;	SOC.W23
61		SD2_D2	GPIO2_IO17	Bank voltage set on SOM 1.8V/3.3V;	SOC.V24
62		SD2_D0	GPIO2_IO15	Bank voltage set on SOM 1.8V/3.3V;	SOC.AB23
63		SD2_D1	GPIO2_IO16	Bank voltage set on SOM 1.8V/3.3V;	SOC.AB24
64		SD2_CMD	GPIO2_IO14	Includes 2.4K PU on SOM to NVCC_SD2_1V8_3V3; Bank voltage set on SOM 1.8V/3.3V;	SOC.W24
65		SD2_D3	GPIO2_IO18	Bank voltage set on SOM 1.8V/3.3V;	SOC.V23
66		GND		Digital Ground	GND
67		GND		Digital Ground	GND
68		SPDIF_RX	GPIO5_IO04		SOC.AG9
69		SPDIF_TX	GPIO5_IO03		SOC.AF9
70		ECSPI2_MOSI	GPIO5_IO11		SOC.B8
71		SD2_RESET_B	GPIO2_IO19	Alt function "SD2_RESET_B" can be used to control the SD card power in order to perform SD RESET function. Bank voltage set on SOM 1.8V/3.3V;	SOC.AB26
72		GPIO1_IO11	GPIO1_IO11		SOC.AC10
73		SAI2_MCLK	GPIO4_IO27		SOC.AD19
74		ENET_MDC	GPIO1_IO16	Shared on SOM with "EC"; Powered by VDD_ENET.	SOC.AC27
75		ECSPI2_SCLK	GPIO5_IO10		SOC.E6

PIN#	ASSY	BALL NAME	GPIO	NOTES	BALL
76		GND		Digital Ground	GND
77		ECSPI2_MISO	GPIO5_IO12		SOC.A8
78		GND		Digital Ground	GND
79		ECSPI2_SS0	GPIO5_IO13		SOC.A6
80		GPIO1_IO10	GPIO1_IO10	Normally used as SD Card Detect for other SOM compatibility.	SOC.AD10
81		GPIO1_IO00	GPIO1_IO00	Used internally with "CN" (CN-FD_CS_B)	SOC.AG14
82		SAI3_TXD	GPIO5_IO01		SOC.AF6
83		UART4_RXD	GPIO5_IO28	Used as debug UART on Variscite base board.	SOC.F19
84		SAI1_RXD1	GPIO4_IO03	Pull down 100K on SOM; Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AF15
85		UART4_TXD	GPIO5_IO29	Used as debug UART on Variscite base board.	SOC.F18
86		SAI1_RXD3	GPIO4_IO05	1K internal PD (not 100K for compatibility to other SOM) Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AF17
87		I2C2_SDA	GPIO5_IO17		SOC.D9
88		I2C2_SCL	GPIO5_IO16		SOC.D10
89		GND		Digital Ground	GND
90		I2C3_SDA	GPIO5_IO19	Used internally with "AC" (Codec I2C) - Do not alter pinmux! 10K internal PU included;	SOC.F10
91		GPIO1_IO15	GPIO1_IO15	Optional interface for MCP2518; See section 8.16.1	SOC.AB9
92		I2C3_SCL	GPIO5_IO18	Used internally with "AC" (Codec I2C) - Do not alter pinmux! 10K internal PU included;	SOC.E10
93		SAI1_TXFS	GPIO4_IO10		SOC.AB19
94		USB1_ID		USB PHY ID pin; No GPIO function.	SOC.D22
95		GND		Digital Ground	GND
96		GPIO1_IO06	GPIO1_IO06		SOC.AG11
97	No EC	ENET_TXC	GPIO1_IO23	Powered by VDD_ENET pin; Includes series EMI filter	SOC.AG24
97	EC	NC		With "EC" configuration this pin in Not Connected.	NC_EC
98		PMIC_PWRON_B		PMIC input to control SOM power rails; PWRON_B is an active-low input for triggering the system to power on or off.	PMIC.40
99		GPIO1_IO14	GPIO1_IO14	Used internally with "TP" (RES-TOUCH_CS_B)	SOC.AC9
100		PCIE1_REF_CLK_N			SOC.A21
101		GND		Digital Ground	GND
102		PCIE1_REF_CLK_P			SOC.B21
103		VCC_SOM		SOM Power	VCC_SOM
104		USB2_VBUS		USB PHY power pin; 5V tolerant	SOC.F23
105		VCC_SOM		SOM Power	VCC_SOM

PIN#	ASSY	BALL NAME	GPIO	NOTES	BALL
106		USB1_VBUS		USB PHY power pin; 5V tolerant	SOC.F22
107		VCC_SOM		SOM Power	VCC_SOM
108		USB2_D_N			SOC.A23
109		VCC_SOM		SOM Power	VCC_SOM
110		USB2_D_P			SOC.B23
111		VCC_SOM		SOM Power	VCC_SOM
112		GND		Digital Ground	GND
113		SAI3_RXFS	GPIO4_IO28		SOC.AG8
114		USB1_D_N			SOC.A22
115		UART2_RXD	GPIO5_IO24		SOC.F15
116		USB1_D_P			SOC.B22
117		GPIO1_IO08	GPIO1_IO08		SOC.AG10
118		GND		Digital Ground	GND
119		CSI_D0_P			SOC.B14
120		SAI3_MCLK	GPIO5_IO02		SOC.AD6
121		CSI_D0_N			SOC.A14
122		GPIO1_IO12	GPIO1_IO12		SOC.AB10
123		CSI_D1_N			SOC.A15
124		UART3_TXD	GPIO5_IO27	Appear on pins 57 & 124 for other SOM modules UART compatibility	SOC.D18
125		CSI_D1_P			SOC.B15
126		GND		Digital Ground	GND
127		CSI_D2_P			SOC.B17
128		PCIE1_TX_N			SOC.A20
129		CSI_D2_N			SOC.A17
130		PCIE1_TX_P			SOC.B20
131		CSI_D3_N			SOC.A18
132		GND		Digital Ground	GND
133		CSI_D3_P			SOC.B18
134		PCIE1_RX_P			SOC.B19
135		CSI_CK_P			SOC.B16
136		PCIE1_RX_N			SOC.A19
137		CSI_CK_N			SOC.A16
138		GND		Digital Ground	GND
139		GND		Digital Ground	GND
140		PMIC_STBY_REQ		SOC output controls the PMIC state; Can be used externally to control carrier board power	SOC.E24
141		SAI1_TXD2	GPIO4_IO14	Driven on SOM during POR_B; Some NAND configuration include 10K pull up; Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AG21
142		PMIC_ON_REQ		SOC output; Controls the PMIC state; Can be used for custom board power control.	SOC.A24

PIN#	ASSY	BALL NAME	GPIO	NOTES	BALL
143		ONOFF		SOC input with internal PU	SOC.A25
144		GND		Digital Ground	GND
145		SAI1_RXD5	GPIO4_IO07	Pull down 100K on SOM; Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AF18
146		SAI1_TXD6	GPIO4_IO18	Pull down 100K on SOM; Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AG23
147		SAI1_TXD0	GPIO4_IO12	Pull down 100K on SOM; Some NAND configuration include 10K pull up; Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AG20
148		SAI1_RXD0	GPIO4_IO02	Pull down 100K on SOM; Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AG15
149		GND		Digital Ground	GND
150		GPIO1_IO03	GPIO1_IO03	Used internally with "TP" (RES-TOUCH_INT_B)	SOC.AF13
151		SAI1_RXD4	GPIO4_IO06	Pull down 100K on SOM; Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AG18
152		SAI1_TXD1	GPIO4_IO13	Pull down 100K on SOM; Some NAND configuration include 10K pull up; Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AF20
153		GPIO1_IO05	GPIO1_IO05	Used internally with "CN" (CAN_INT_B)	SOC.AF12
154		GPIO1_IO01	GPIO1_IO01		SOC.AF14
155		SAI1_TXD5	GPIO4_IO17	Driven on SOM during POR_B; Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AF22
156		SAI1_TXD7	GPIO4_IO19	Pull down 100K on SOM; Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AF23
157		SAI1_RXD6	GPIO4_IO08	Pull down 100K on SOM; Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AG19
158		GND		Digital Ground	GND
159		GND		Digital Ground	GND
160	No LD	DSI_D1_N			SOC.A10
160	LD	LVDS0_CH0_TX1_N		Signal source is LVDS Bridge.	SN65DSI84.D9
161	No LD	DSI_D0_N			SOC.A9
161	LD	LVDS0_CH0_TX0_N		Signal source is LVDS Bridge.	SN65DSI84.C9
162	No LD	DSI_D1_P			SOC.B10
162	LD	LVDS0_CH0_TX1_P		Signal source is LVDS Bridge.	SN65DSI84.D8

PIN#	ASSY	BALL NAME	GPIO	NOTES	BALL
163	No LD	DSI_D0_P			SOC.B9
163	LD	LVDS0_CH0_TX0_P		Signal source is LVDS Bridge.	SN65DSI84.C8
164	No LD	DSI_D2_N			SOC.A12
164	LD	LVDS0_CH0_TX2_N		Signal source is LVDS Bridge.	SN65DSI84.E9
165	No LD	DSI_D3_N			SOC.A13
165	LD	LVDS0_CH0_TX3_N		Signal source is LVDS Bridge.	SN65DSI84.G9
166	No LD	DSI_D2_P			SOC.B12
166	LD	LVDS0_CH0_TX2_P		Signal source is LVDS Bridge.	SN65DSI84.E8
167	No LD	DSI_D3_P			SOC.B13
167	LD	LVDS0_CH0_TX3_P		Signal source is LVDS Bridge.	SN65DSI84.G8
168	No LD	DSI_CLK_N			SOC.A11
168	LD	LVDS0_CH0_CLK_N		Signal source is LVDS Bridge.	SN65DSI84.F9
169		GND		Digital Ground	GND
170	No LD	DSI_CLK_P			SOC.B11
170	LD	LVDS0_CH0_CLK_P		Signal source is LVDS Bridge.	SN65DSI84.F8
171		UART2_TXD	GPIO5_IO25		SOC.E15
172		GND		Digital Ground	GND
173		SAI1_TXD3	GPIO4_IO15	Driven on SOM during POR_B; Some NAND configuration include 10K pull down; Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AF21
174		I2C4_SCL	GPIO5_IO20		SOC.D13
175		UART3_RXD	GPIO5_IO26	Appear on pins 55 & 175 for other SOM modules UART compatibility	SOC.E18
176		I2C4_SDA	GPIO5_IO21		SOC.E13
177		SAI1_TXC	GPIO4_IO11		SOC.AC18
178		GND		Digital Ground	GND
179		GND		Digital Ground	GND
180	No LD	NC		Pin not connected with No "LD" configuration!	NC_No_LD
180	LD	LVDS0_CH1_CLK_N		Signal source is LVDS Bridge.	SN65DSI84.A6
181	No LD	NC		Pin not connected with No "LD" configuration!	NC_No_LD
181	LD	LVDS0_CH1_TX3_P		Signal source is LVDS Bridge.	SN65DSI84.B7
182	No LD	NC		Pin not connected with No "LD" configuration!	NC_No_LD
182	LD	LVDS0_CH1_CLK_P		Signal source is LVDS Bridge.	SN65DSI84.B6
183	No LD	NC		Pin not connected with No "LD" configuration!	NC_No_LD
183	LD	LVDS0_CH1_TX3_N		Signal source is LVDS Bridge.	SN65DSI84.A7
184	No LD	NC		Pin not connected with No "LD" configuration!	NC_No_LD
184	LD	LVDS0_CH1_TX0_N		Signal source is LVDS Bridge.	SN65DSI84.A3
185		GND		Digital Ground	GND
186	No LD	NC		Pin not connected with No "LD" configuration!	NC_No_LD
186	LD	LVDS0_CH1_TX0_P		Signal source is LVDS Bridge.	SN65DSI84.B3

PIN#	ASSY	BALL NAME	GPIO	NOTES	BALL
187	No TP	SAI1_RXD2	GPIO4_IO04	Exposed with no "TP" configuration: Pull down 100K on SOM Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AG17
187	TP	TS_X-		Signal source is Resistive Touch controller.	TSC2046.8
188	No LD	NC		Pin not connected with No "LD" configuration!	NC_No_LD
188	LD	LVDS0_CH1_TX1_N		Signal source is LVDS Bridge.	SN65DSI84.A4
189	No TP	SAI1_MCLK	GPIO4_IO20	Exposed with no "TP" configuration	SOC.AB18
189	TP	TS_X+		Signal source is Resistive Touch controller.	TSC2046.6
190	No LD	NC		Pin not connected with No "LD" configuration!	NC_No_LD
190	LD	LVDS0_CH1_TX1_P		Signal source is LVDS Bridge.	SN65DSI84.B4
191	No TP	SAI1_RXFS	GPIO4_IO00	Exposed with no "TP" configuration	SOC.AG16
191	TP	TS_Y+		Signal source is Resistive Touch controller.	TSC2046.7
192	No LD	NC		Pin not connected with No "LD" configuration!	NC_No_LD
192	LD	LVDS0_CH1_TX2_N		Signal source is LVDS Bridge.	SN65DSI84.A5
193	No TP	SAI1_RXC	GPIO4_IO01	Exposed with no "TP" configuration	SOC.AF16
193	TP	TS_Y-		Signal source is Resistive Touch controller.	TSC2046.9
194	No LD	NC		Pin not connected with No "LD" configuration!	NC_No_LD
194	LD	LVDS0_CH1_TX2_P		Signal source is LVDS Bridge.	SN65DSI84.B5
195		AGND		Audio Ground	AGND
196	No AC	SAI5_RXFS	GPIO3_IO19	With “AC” configuration do not alter PINMUX function.	SOC.AB15
196	AC	HPOUTFB		Signal source is Audio Codec.	WM8904.14
197	No AC	SAI5_RXC	GPIO3_IO20	With “AC” configuration do not alter PINMUX function.	SOC.AC15
197	AC	LINEIN1_LP		Signal source is Audio Codec.	WM8904.26
198	No AC	SAI5_RXD0	GPIO3_IO21	With “AC” configuration do not alter PINMUX function.	SOC.AD18
198	AC	HPLOUT		Signal source is Audio Codec.	WM8904.13
199	No AC	SAI5_RXD1	GPIO3_IO22	With “AC” configuration do not alter PINMUX function.	SOC.AC14
199	AC	LINEIN1_RP		Signal source is Audio Codec.	WM8904.24
200	No AC	SAI5_RXD2	GPIO3_IO23	With “AC” configuration do not alter PINMUX function.	SOC.AD13
200	AC	HPROUT		Signal source is Audio Codec.	WM8904.15

7.4. VAR-SOM-MX8M-MINI Pin-Mux

This section tables lists the SOM connectors with the available functions on each pin.

Table 4: VAR-SOM-MX8M-MINI PINMUX

PIN	ASSY	BALL	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6
1	No EC	SOC.AF24	ENET_TX_CTL					GPIO1_IO22	
3	No EC	SOC.AF25	ENET_TD3					GPIO1_IO18	
4	No EC	SOC.AE27	ENET_RD0					GPIO1_IO26	
5	No EC	SOC.AG25	ENET_TD2	IN=ENET_TX_CLK OUT=ENET_REF_CLK_ROOT				GPIO1_IO19	
6	No EC	SOC.AD27	ENET_RD1					GPIO1_IO27	
9	No EC	SOC.AF26	ENET_TD1					GPIO1_IO20	
10	No EC	SOC.AD26	ENET_RD2					GPIO1_IO28	
11	No EC	SOC.AG26	ENET_TD0					GPIO1_IO21	
12	No EC	SOC.AC26	ENET_RD3					GPIO1_IO29	
15	No EC	SOC.AF27	ENET_RX_CTL					GPIO1_IO24	
16	No EC	SOC.AE26	ENET_RXC	ENET_RX_ER				GPIO1_IO25	
17		SOC.AF8	SPDIF_EXT_CLK	PWM1_OUT				GPIO5_IO05	
18	No AC	SOC.AC13	SAI5_RXD3	SAI1_TXD5	SAI1_TXFS	SAI5_TXD0	PDM_BIT3	GPIO3_IO24	
20	No AC	SOC.AD15	SAI5_MCLK	SAI1_TXC				GPIO3_IO25	
21		SOC.AC24	SAI2_RXD0	SAI5_TXD0			UART1_RTS_B	GPIO4_IO23	
22		SOC.AB22	SAI2_RXC	SAI5_TXC			UART1_RXD	GPIO4_IO22	
23		SOC.AC19	SAI2_RXFS	SAI5_TXFS	SAI5_TXD1	SAI2_RXD1	UART1_TXD	GPIO4_IO21	
24		SOC.AD23	SAI2_TXFS	SAI5_TXD1		SAI2_TXD1	UART1_CTS_B	GPIO4_IO24	
25		SOC.AD22	SAI2_TXC	SAI5_TXD2				GPIO4_IO25	
26		SOC.AC22	SAI2_TXD0	SAI5_TXD3				GPIO4_IO26	
29		SOC.AF11	GPIO1_IO07	ENET_MDIO					EXT_CLK4
30		SOC.AB27	ENET_MDIO					GPIO1_IO17	
39		SOC.B6	ECSPI1_SS0	UART3_RTS_B				GPIO5_IO09	
40		SOC.AD9	GPIO1_IO13	USB1_OTG_OC				PWM2_OUT	

PIN	ASSY	BALL	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6
41		SOC.A7	ECSPI1_MISO	UART3_CTS_B				GPIO5_IO08	
43		SOC.D6	ECSPI1_SCLK	UART3_RXD				GPIO5_IO06	
45		SOC.B7	ECSPI1_MOSI	UART3_TXD				GPIO5_IO07	
48		SOC.AG13	GPIO1_IO02	WDOG_B				WDOG_ANY	
50		SOC.AG7	SAI3_RXC	GPT1_CLK	SAI5_RXC		UART2_CTS_B	GPIO4_IO29	
51		SOC.AF7	SAI3_RXD	GPT1_COMPARE1	SAI5_RXD0		UART2_RTS_B	GPIO4_IO30	
52		SOC.AG6	SAI3_TXC	GPT1_COMPARE2	SAI5_RXD2		UART2_TXD	GPIO5_IO00	
53		SOC.AC6	SAI3_TXFS	GPT1_CAPTURE2	SAI5_RXD1	SAI3_TXD1	UART2_RXD	GPIO4_IO31	
54		SOC.E14	UART1_RXD	ECSPI3_SCLK				GPIO5_IO22	
55		SOC.E18	UART3_RXD	UART1_CTS_B				GPIO5_IO26	
56		SOC.F13	UART1_TXD	ECSPI3_MOSI				GPIO5_IO23	
57		SOC.D18	UART3_TXD	UART1_RTS_B				GPIO5_IO27	
60		SOC.W23	SD2_CLK					GPIO2_IO13	
61		SOC.V24	SD2_DATA2					GPIO2_IO17	
62		SOC.AB23	SD2_DATA0					GPIO2_IO15	
63		SOC.AB24	SD2_DATA1					GPIO2_IO16	
64		SOC.W24	SD2_CMD					GPIO2_IO14	
65		SOC.V23	SD2_DATA3					GPIO2_IO18	
68		SOC.AG9	SPDIF_RX	PWM2_OUT				GPIO5_IO04	
69		SOC.AF9	SPDIF_TX	PWM3_OUT				GPIO5_IO03	
70		SOC.B8	ECSPI2_MOSI	UART4_TXD				GPIO5_IO11	
71		SOC.AB26	SD2_RESET_B					GPIO2_IO19	
72		SOC.AC10	GPIO1_IO11	USB2_OTG_ID					
73		SOC.AD19	SAI2_MCLK	SAI5_MCLK				GPIO4_IO27	
74		SOC.AC27	ENET_MDC					GPIO1_IO16	
75		SOC.E6	ECSPI2_SCLK	UART4_RXD				GPIO5_IO10	
77		SOC.A8	ECSPI2_MISO	UART4_CTS_B				GPIO5_IO12	
79		SOC.A6	ECSPI2_SS0	UART4_RTS_B				GPIO5_IO13	
80		SOC.AD10	GPIO1_IO10	USB1_OTG_ID					
81		SOC.AG14	GPIO1_IO00	ENET_PHY_REF_CLK_ROOT_OUT				REF_CLK_32K	EXT_CLK1
82		SOC.AF6	SAI3_TXD	GPT1_COMPARE3	SAI5_RXD3			GPIO5_IO01	

PIN	ASSY	BALL	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6
83		SOC.F19	UART4_RXD	UART2_CTS_B	PCIE1_CLKREQ_B			GPIO5_IO28	
84		SOC.AF15	SAI1_RXD1	SAI5_RXD1		PDM_BIT1		GPIO4_IO03	BOOT_CFG01
85		SOC.F18	UART4_TXD	UART2_RTS_B				GPIO5_IO29	
86		SOC.AF17	SAI1_RXD3	SAI5_RXD3		PDM_BIT3		GPIO4_IO05	BOOT_CFG03
87		SOC.D9	I2C2_SDA	ENET_1588_EVENT1_OUT				GPIO5_IO17	
88		SOC.D10	I2C2_SCL	ENET_1588_EVENT1_IN				GPIO5_IO16	
90		SOC.F10	I2C3_SDA	PWM3_OUT	GPT3_CLK			GPIO5_IO19	
91		SOC.AB9	GPIO1_IO15	USB2_OTG_OC				PWM4_OUT	CLKO2
92		SOC.E10	I2C3_SCL	PWM4_OUT	GPT2_CLK			GPIO5_IO18	
93		SOC.AB19	SAI1_TXFS	SAI5_TXFS				GPIO4_IO10	
94		SOC.D22	USB1_ID						
96		SOC.AG11	GPIO1_IO06	ENET_MDC				SD1_CD_B	EXT_CLK3
97	No EC	SOC.AG24	ENET_TXC	ENET_TX_ER				GPIO1_IO23	
99		SOC.AC9	GPIO1_IO14	USB2_OTG_PWR				PWM3_OUT	CLKO1
113		SOC.AG8	SAI3_RXFS	GPT1_CAPTURE1	SAI5_RXFS	SAI3_RXD1		GPIO4_IO28	
115		SOC.F15	UART2_RXD	ECSPI3_MISO				GPIO5_IO24	
117		SOC.AG10	GPIO1_IO08	ENET_1588_EVENT0_IN				SD2_RESET_B	
120		SOC.AD6	SAI3_MCLK	PWM4_OUT	SAI5_MCLK			GPIO5_IO02	
122		SOC.AB10	GPIO1_IO12	USB1_OTG_PWR					
124		SOC.D18	UART3_TXD	UART1_RTS_B				GPIO5_IO27	
141		SOC.AG21	SAI1_TXD2	SAI5_TXD2				GPIO4_IO14	BOOT_CFG10
145		SOC.AF18	SAI1_RXD5	SAI6_TXD0	SAI6_RXD0	SAI1_RXFS		GPIO4_IO07	BOOT_CFG05
146		SOC.AG23	SAI1_TXD6	SAI6_RXFS	SAI6_TXFS			GPIO4_IO18	BOOT_CFG14
147		SOC.AG20	SAI1_TXD0	SAI5_TXD0				GPIO4_IO12	BOOT_CFG08
148		SOC.AG15	SAI1_RXD0	SAI5_RXD0	SAI1_TXD1	PDM_BIT0		GPIO4_IO02	BOOT_CFG00
150		SOC.AF13	GPIO1_IO03	USDHC1_VSELECT					

PIN	ASSY	BALL	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6
151		SOC.AG18	SAI1_RXD4	SAI6_TXC	SAI6_RXC			GPIO4_IO06	BOOT_CFG04
152		SOC.AF20	SAI1_TXD1	SAI5_TXD1				GPIO4_IO13	BOOT_CFG09
153		SOC.AF12	GPIO1_IO05	M4_NMI				PMIC_READY	
154		SOC.AF14	GPIO1_IO01	PWM1_OUT				REF_CLK_24M	EXT_CLK2
155		SOC.AF22	SAI1_TXD5	SAI6_RXD0	SAI6_TXD0			GPIO4_IO17	BOOT_CFG13
156		SOC.AF23	SAI1_TXD7	SAI6_MCLK		PDM_CLK		GPIO4_IO19	BOOT_CFG15
157		SOC.AG19	SAI1_RXD6	SAI6_TXFS	SAI6_RXFS			GPIO4_IO08	BOOT_CFG06
171		SOC.E15	UART2_TXD	ECSPI3_SS0				GPIO5_IO25	
173		SOC.AF21	SAI1_TXD3	SAI5_TXD3				GPIO4_IO15	BOOT_CFG11
174		SOC.D13	I2C4_SCL	PWM2_OUT	PCIE1_CLKREQ_B			GPIO5_IO20	
175		SOC.E18	UART3_RXD	UART1_CTS_B				GPIO5_IO26	
176		SOC.E13	I2C4_SDA	PWM1_OUT				GPIO5_IO21	
177		SOC.AC18	SAI1_TXC	SAI5_TXC				GPIO4_IO11	
187	No TP	SOC.AG17	SAI1_RXD2	SAI5_RXD2		PDM_BIT2		GPIO4_IO04	BOOT_CFG02
189	No TP	SOC.AB18	SAI1_MCLK	SAI5_MCLK	SAI1_TXC	PDM_CLK		GPIO4_IO20	
191	No TP	SOC.AG16	SAI1_RXFS	SAI5_RXFS				GPIO4_IO00	
193	No TP	SOC.AF16	SAI1_RXC	SAI5_RXC				GPIO4_IO01	
196	No AC	SOC.AB15	SAI5_RXFS	SAI1_TXD0				GPIO3_IO19	
197	No AC	SOC.AC15	SAI5_RXC	SAI1_TXD1			PDM_CLK	GPIO3_IO20	
198	No AC	SOC.AD18	SAI5_RXD0	SAI1_TXD2			PDM_BIT0	GPIO3_IO21	
199	No AC	SOC.AC14	SAI5_RXD1	SAI1_TXD3	SAI1_TXFS	SAI5_TXFS	PDM_BIT1	GPIO3_IO22	
200	No AC	SOC.AD13	SAI5_RXD2	SAI1_TXD4	SAI1_TXFS	SAI5_TXC	PDM_BIT2	GPIO3_IO23	

8. SOM's Interfaces

8.1. Acronyms Used for Interface Tables

Acronym used in the tables listed under this section:

Table 5: Interface Tables Mnemonics

Column Heading		Meaning
PIN#		Pin number on a connector: Can be 1 to 200
ALT NAME		Pin type & direction
ALT#		Alternate number for the function. Blank in case the function origin is a PHY pin.
NOTES		This column displays any special note related to the specific pin with the specific ASSY.
BALL	**XX.YY**	Source device and its pin number; See Table 2.

8.2. Trace Impedance

SOM traces are designed with the below table impedance list per signal group.
Table is a reference when you are updating or creating constraints in the PCB design tool to set up the impedances/trace widths.

Table 6: SOM Signal Group Traces Impedance

Signal Group	Impedance
All single ended signals	50 Ω Single ended
PCIe TX/RX data pairs	85 Ω Differential
USB Differential signals	90 Ω Differential
Differential signals including: Ethernet, PCIe clocks, MIPI (CSI and DSI), LVDS lines	100 Ω Differential

8.3. Display Interfaces

The VAR-SOM-MX8M-MINI consists of the following display interfaces options:

- MIPI DSI – **No *"LD" Configuration***
  - MIPI-DSI standard v1.1 support resolution up to 1920x1080p60.
  - Up to 4 data lanes support D-PHY
  - 80Mbps - 1.5Gbps data rate in high speed operation
  - 10Mbps data rate in low power operation
  - Implements all three DSI Layers (Pixel to Byte packing, Low Level Protocol, Lane Management)
  - Supports High Speed and Low Power operation
  - Host Version
- LVDS - ***"LD" Configuration***
  - Implemented using SN65DSI84 (see section 5.6)
  - Support single channel DSI to Single-Link or Dual-Link "FLATLINK" LVDS output format.
  - Resolution up to 1920x1200 60 fps at 24 bpp/18 bpp, but limited by the DSI interface to 1920x1080.
  - DSI Channel has 4 DSI data lanes + 1 CLK lane.
  - Each LVDS link has 4 data lanes + 1 CLK lane.

8.3.1. MIPI-DSI Signals

The MIPI-DSI signals share the same pins as the LVDS channel 2 function depending on the orderable configuration option.

Table 7: MIPI-DSI Signals

PIN#	ASSY	ALT NAME	ALT#	NOTES	BALL
168	No LD	MIPI_DSI_CLK_N	0	Differential Pair Negative side	SOC.A11
170	No LD	MIPI_DSI_CLK_P	0	Differential Pair Positive side	SOC.B11
161	No LD	MIPI_DSI_TX0_N	0	Differential Pair Negative side	SOC.A9
163	No LD	MIPI_DSI_TX0_P	0	Differential Pair Positive side	SOC.B9
160	No LD	MIPI_DSI_TX1_N	0	Differential Pair Negative side	SOC.A10
162	No LD	MIPI_DSI_TX1_P	0	Differential Pair Positive side	SOC.B10
164	No LD	MIPI_DSI_TX2_N	0	Differential Pair Negative side	SOC.A12
166	No LD	MIPI_DSI_TX2_P	0	Differential Pair Positive side	SOC.B12
165	No LD	MIPI_DSI_TX3_N	0	Differential Pair Negative side	SOC.A13
167	No LD	MIPI_DSI_TX3_P	0	Differential Pair Positive side	SOC.B13

8.3.2. LVDS Display Signals

The LVDS display output support includes two channels generated by the driving IC, see section 5.6.

Sections 8.3.2.1 and 0 lists the interface pins and signal description.

8.3.2.1. LVDS Display Signals Channel 0

Table 8: LVDS Display Channel 0 Signals

PIN#	ASSY	ALT NAME	ALT#	NOTES	BALL
168	LD	LVDS0_CH0_CLK_N		Differential Pair Negative side Signal source is LVDS Bridge.	SN65DSI84.F9
170	LD	LVDS0_CH0_CLK_P		Differential Pair Positive side Signal source is LVDS Bridge.	SN65DSI84.F8
161	LD	LVDS0_CH0_TX0_N		Differential Pair Negative side Signal source is LVDS Bridge.	SN65DSI84.C9
163	LD	LVDS0_CH0_TX0_P		Differential Pair Positive side Signal source is LVDS Bridge.	SN65DSI84.C8
160	LD	LVDS0_CH0_TX1_N		Differential Pair Negative side Signal source is LVDS Bridge.	SN65DSI84.D9
162	LD	LVDS0_CH0_TX1_P		Differential Pair Positive side Signal source is LVDS Bridge.	SN65DSI84.D8
164	LD	LVDS0_CH0_TX2_N		Differential Pair Negative side Signal source is LVDS Bridge.	SN65DSI84.E9
166	LD	LVDS0_CH0_TX2_P		Differential Pair Positive side Signal source is LVDS Bridge.	SN65DSI84.E8
165	LD	LVDS0_CH0_TX3_N		Differential Pair Negative side Signal source is LVDS Bridge.	SN65DSI84.G9
167	LD	LVDS0_CH0_TX3_P		Differential Pair Positive side Signal source is LVDS Bridge.	SN65DSI84.G8

NOTE

When the ***"LD" configuration*** NOT chosen, the LVDS Channel 0 pins exposes the MIPI-DSI on the VAR-SOM-MX8M-MINI connector.

8.3.2.2. LVDS Display Signals Channel 1

Table 9: LVDS Display Channel 1 Signals

PIN#	ASSY	ALT NAME	ALT#	NOTES	BALL
180	LD	LVDS0_CH1_CLK_N		Differential Pair Negative side Signal source is LVDS Bridge.	SN65DSI84.A6
182	LD	LVDS0_CH1_CLK_P		Differential Pair Positive side Signal source is LVDS Bridge.	SN65DSI84.B6
184	LD	LVDS0_CH1_TX0_N		Differential Pair Negative side Signal source is LVDS Bridge.	SN65DSI84.A3
186	LD	LVDS0_CH1_TX0_P		Differential Pair Positive side Signal source is LVDS Bridge.	SN65DSI84.B3
188	LD	LVDS0_CH1_TX1_N		Differential Pair Negative side Signal source is LVDS Bridge.	SN65DSI84.A4
190	LD	LVDS0_CH1_TX1_P		Differential Pair Positive side Signal source is LVDS Bridge.	SN65DSI84.B4
192	LD	LVDS0_CH1_TX2_N		Differential Pair Negative side Signal source is LVDS Bridge.	SN65DSI84.A5
194	LD	LVDS0_CH1_TX2_P		Differential Pair Positive side Signal source is LVDS Bridge.	SN65DSI84.B5
183	LD	LVDS0_CH1_TX3_N		Differential Pair Negative side Signal source is LVDS Bridge.	SN65DSI84.A7
181	LD	LVDS0_CH1_TX3_P		Differential Pair Positive side Signal source is LVDS Bridge.	SN65DSI84.B7

8.4. Camera Interface

8.4.1. MIPI Camera Serial Interface

The CSI-2 Host Controller is a digital core that implements all protocol functions defined in the MIPI CSI-2 specification, providing an interface between the system and the MIPI D-PHY, allowing communication with an MIPI CSI-2 compliant camera sensor.

Key features include:

- Module provides one four-lane MIPI camera serial interfaces
- MIPI D-PHY specification V1.2 (Board Approved)
- Compliant to MIPI CSI2 Specification V1.3 except for C-PHY feature (Board Approved)
- Support primary and secondary Image format
    - YUV420, YUV420 (Legacy), YUV420 (CSPS), YUV422 of 8-bits and 10-bits
    - RGB565, RGB666, RGB888
    - RAW6, RAW7, RAW8, RAW10, RAW12, RAW14
    - All of User defined Byte-based Data packet
- Support up to 4 lanes of D-PHY, which operates up to a maximum bit rate of 1.5 Gbps.
- Interfaces
    - Compatible to PPI (Protocol-to-PHY Interface) in MIPI D-PHY Specification
    - AMBA3.0 APB Slave for Register configuration.
    - Image output data bus width: 32 bits
- Image memory
    - Size of SRAM is 4KB
- Pixel clock can be gated when no PPI data is coming

8.4.2. MIPI-CSI2 Signals

The VAR-SOM-MX8M-MINI exposes one MIPI-CSI input port of the i.MX 8M Mini SOC.
The following table list the interface pinout for MIPI-CSI port.

8.4.2.1. MIPI-CSI2 Port 1 Signals

Table 10: MIPI-CSI2 P1 Signals

PIN#	ASSY	ALT NAME	ALT#	NOTES	BALL
137		MIPI_CSI1_CLK_N	0	Differential Pair Negative side	SOC.A16
135		MIPI_CSI1_CLK_P	0	Differential Pair Positive side	SOC.B16
121		MIPI_CSI1_D0_N	0	Differential Pair Negative side	SOC.A14
119		MIPI_CSI1_D0_P	0	Differential Pair Positive side	SOC.B14
123		MIPI_CSI1_D1_N	0	Differential Pair Negative side	SOC.A15
125		MIPI_CSI1_D1_P	0	Differential Pair Positive side	SOC.B15
129		MIPI_CSI1_D2_N	0	Differential Pair Negative side	SOC.A17
127		MIPI_CSI1_D2_P	0	Differential Pair Positive side	SOC.B17
131		MIPI_CSI1_D3_N	0	Differential Pair Negative side	SOC.A18
133		MIPI_CSI1_D3_P	0	Differential Pair Positive side	SOC.B18

8.5. Ethernet Interface

The VAR-SOM-MX8M-MINI exposes two **optional** interfaces on the same pins depending on the configuration:

- MDI lines driven by the AR8033/ADIN1300 Gigabit PHY – ***"EC" Configuration***
- ENET signal driven by the SOC – **No *"EC" Configuration***

The SOC core implements a triple-speed 10/100/1000-Mbit/s Ethernet MACs compliant with the IEEE802.3-2002 standard.

The i.MX8M processor also consists of HW support for **IEEE1588** standard.

8.5.1. Ethernet PHY

The on-SOM Gigabit Ethernet PHY in conjunction with external magnetics on carrier board complete the interface to the media.

8.5.1.1. Gigabit Ethernet Signals

Table 11: Ethernet PHY Signals

PIN#	ASSY	ALT NAME	ALT#	NOTES	BALL
15	EC	ETH_LED_ACT		Signal source is Ethernet PHY.	AR8033.23/ ADIN1300.21
16	EC	ETH_LED_LINK10_100_1000		Signal source is Ethernet PHY.	AR8033.24_26/ ADIN1300.26 via inv. FET
5	EC	ETH_TRX0_N		Differential Pair Negative side Signal source is Ethernet PHY.	AR8033.12/ ADIN1300.13
3	EC	ETH_TRX0_P		Differential Pair Positive side Signal source is Ethernet PHY.	AR8033.11/ ADIN1300.12
11	EC	ETH_TRX1_N		Differential Pair Negative side Signal source is Ethernet PHY.	AR8033.15/ ADIN1300.15
9	EC	ETH_TRX1_P		Differential Pair Positive side Signal source is Ethernet PHY.	AR8033.14/ ADIN1300.14
6	EC	ETH_TRX2_N		Differential Pair Negative side Signal source is Ethernet PHY.	AR8033.18/ ADIN1300.17
4	EC	ETH_TRX2_P		Differential Pair Positive side Signal source is Ethernet PHY.	AR8033.17/ ADIN1300.16
12	EC	ETH_TRX3_N		Differential Pair Negative side Signal source is Ethernet PHY.	AR8033.21/ ADIN1300.19
10	EC	ETH_TRX3_P		Differential Pair Positive side Signal source is Ethernet PHY.	AR8033.20/ ADIN1300.18
1	EC	ETH_NC		With "EC" configuration this pin in Not Connected.	NC_EC

Table 12: AR8033 Ethernet PHY LED Behavior

Symbol	10M link	10M active	100M link	100M active	1000M link	1000M active
LED_10_100_1000	OFF	OFF	ON	ON	ON	ON
LED_ACT	ON	BLINK	ON	BLINK	ON	BLINK
ON = active; OFF = inactive						

Table 13: ADIN1300 Ethernet PHY LED Behavior

Symbol	10M link	10M active	100M link	100M active	1000M link	1000M active
LED_10_100_1000	ON	ON	ON	ON	ON	ON
LED_ACT	ON	BLINK	ON	BLINK	ON	BLINK
ON = active; OFF = inactive						

8.5.2. 10/100/1000Mbps Ethernet MAC(ENET) Signals

Table 14: ENET Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
4	No EC	ENET_RD0	0	Powered by VDD_ENET pin RGMII Data in	SOC.AE27
6	No EC	ENET_RD1	0	Powered by VDD_ENET pin RGMII Data in	SOC.AD27
10	No EC	ENET_RD2	0	Powered by VDD_ENET pin RGMII Data in	SOC.AD26
12	No EC	ENET_RD3	0	Powered by VDD_ENET pin RGMII Data in	SOC.AC26
15	No EC	ENET_RX_CTL	0	Powered by VDD_ENET pin RGMII Receive data Control	SOC.AF27
16	No EC	ENET_RX_ER	1	Powered by VDD_ENET pin; Includes series EMI filter ENET RGMII Receive Clock: 125MHz @ 1000Mbps / 25MHz @ 100Mbps / 2.5MHz @ 10Mbps Samples RD[3:0] and RX_CTL	SOC.AE26
16	No EC	ENET_RXC	0	Powered by VDD_ENET pin; Includes series EMI filter ENET RGMII Receive Clock: 125MHz @ 1000Mbps / 25MHz @ 100Mbps / 2.5MHz @ 10Mbps Samples RD[3:0] and RX_CTL	SOC.AE26
11	No EC	ENET_TD0	0	Powered by VDD_ENET pin RGMII Data out	SOC.AG26
9	No EC	ENET_TD1	0	Powered by VDD_ENET pin RGMII Data out	SOC.AF26
5	No EC	ENET_TD2	0	Powered by VDD_ENET pin RGMII Data out	SOC.AG25
3	No EC	ENET_TD3	0	Powered by VDD_ENET pin RGMII Data out	SOC.AF25
1	No EC	ENET_TX_CTL	0	Powered by VDD_ENET pin; On some SOM modules this pin is GND; If placed in such carrier with no "EC" configuration define PAD as input! RGMII Transmit data Control	SOC.AF24
97	No EC	ENET_TX_ER	1	Powered by VDD_ENET pin; Includes series EMI filter ENET RGMII Transmit Clock: 125MHz @ 1000Mbps / 25MHz @ 100Mbps / 2.5MHz @ 10Mbps Samples TD [3:0] and TX_CTL	SOC.AG24
97	No EC	ENET_TXC	0	Powered by VDD_ENET pin; Includes series EMI filter ENET RGMII Transmit Clock: 125MHz @ 1000Mbps / 25MHz @ 100Mbps / 2.5MHz @ 10Mbps Samples TD [3:0] and TX_CTL	SOC.AG24

8.5.3. MDIO, 1588 & Clock Signals

Table 15: MDIO, 1588 & Clock Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
117		ENET_1588_EVENT0_IN	1		SOC.AG10
88		ENET_1588_EVENT1_IN	1		SOC.D10
87		ENET_1588_EVENT1_OUT	1		SOC.D9
74		ENET_MDC	0	Shared on SOM with "EC"; Powered by VDD_ENET. Do not alter pinmux with "EC" configuration	SOC.AC27
96		ENET_MDC	1		SOC.AG11
29		ENET_MDIO	1		SOC.AF11
30		ENET_MDIO	0	Shared on SOM with "EC"; Includes 1.5K Ohm PU to VDD_ENET; Do not alter pinmux with "EC" configuration	SOC.AB27
81		ENET_PHY_REF_CLK_ROOT_OUT	1	Used internally with "CN" (CN-FD_CS_B) Always exposed	SOC.AG14
5	No EC	IN=ENET_TX_CLK OUT=ENET_REF_CLK_ROOT	1	Powered by VDD_ENET pin RGMII Data out	SOC.AG25
38	No EC	VDD_ENET	0	ENET pins group power IN "EC" configuration: * Not Connected No "EC" configuration: Must supply one option (Max. 50mA required) - * RMII uses 1.8 or 3.3V. * RGMII uses 1.8 or 2.5V. * GPIO 1.8V/2.5V/3.3V	SOC.W22

8.6. Wi-Fi & BT

The VAR-SOM-MX8M-MINI contains a certified high-performance Wi-Fi (Single or Dual Band option) and Bluetooth (BT) module:

- IEEE 802.11 ac/a/b/g/n (Dual Band Option)
- IEEE 802.11 b/g/n (Single Band Option)
- Bluetooth 2.1+EDR
- BLE 5.2 capabilities
- Modules have an antenna connection through a U. FL JACK connector
- Antenna cable connected to module must have 50-Ω impedance

Figure 3 illustrates the VAR-SOM-MX8M-MINI internal Wi-Fi and BT connectivity.

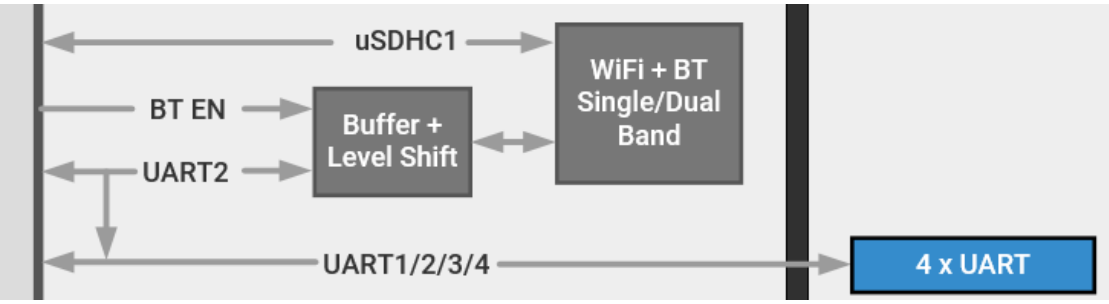


Figure 3: VAR-SOM-MX8M-MINI Wi-Fi & BT Internal Connection

To allow the most flexible solution the following elements are added to the VAR-SOM-MX8M-MINI:

- Buffer with tristate on the BT link based on UART interface.
  Will allow isolation from the BT module and the use by external circuity via the VAR-SOM-MX8M-MINI connector.
- Dedicated uSDHC channel for the Wi-Fi module interface.

NOTE

BT UART tristate buffer controlled using GPIO2_IO06.

- Logic “High” enables the buffer
- Logic “Low” disable it and releases the signals to be used via SOM connector.

8.6.1. Interface Implementation Options

8.6.1.1. Module Configuration **with "WBD"** or **"WB"** Option

- System use: **Wi-Fi and Bluetooth**.
  - BT UART external interface pins should be left floating.
- System use: **Wi-Fi and no BT**.
  - In this case, disable the BT buffer (using GPIO2_IO06) and BT function.
  - BT UART interface pins can be used externally with any of the alternate functions.
- System use: **BT and no Wi-Fi**.
  - Disable Wi-Fi function.
  - Enable the BT buffer (using GPIO2_IO06) and BT function.

8.6.1.2. Module Configuration **without "WBD"** or **"WB"** Option

- System use: No Wi-Fi and no BT.
  - BT UART interface accessible externally with any of its alternative functions.

8.6.2. Bluetooth Interface Signals

Table 16: BT UART interface signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
50		UART2_CTS_B	4	Used internally with "WBD"; Function can be released if BT Buffer disabled. Always exposed;	SOC.AG7
51		UART2_RTS_B	4	Used internally with "WBD"; Function can be released if BT Buffer disabled. Always exposed;	SOC.AF7
53		UART2_RXD	4	Used internally with "WBD"; Function can be released if BT Buffer disabled. Always exposed;	SOC.AC6
52		UART2_TXD	4	Used internally with "WBD"; Function can be released if BT Buffer disabled. Always exposed;	SOC.AG6

8.7. MMC/SD/SDIO

The VAR-SOM-MX8M-MINI exposes uSDHC2 interface of the i.MX 8M Mini SOC.
The following table list the interface pinout for SD1 signals.

The exposed uSDHC controller SD2 can support up to a 4-bit interface designed to support:

- SD/SDIO standard, up to version 3.0.
- MMC standard, up to version 5.0.
- 1.8 V and 3.3 V operation. Does not support 1.2 V operation
- 1-bit/4-bit SD and SDIO modes, 1-bit/4-bit MMC mode
- Up to SDR104 rate

8.7.1. SD1 Signals

The uSDHC controller (SD1) is used internally for the Wi-Fi interface on the SOM.

8.7.2. SD2 Signals

Card Detect function any GPIO can be used; For other SOM compatibility pin 80 GPIO1_IO10 is used for card detect.

Table 17: SD2 interface signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
60		SD2_CLK	0	Bank voltage set on SOM 1.8V/3.3V;	SOC.W23
64		SD2_CMD	0	Includes 2.4K PU on SOM to NVCC_SD2_1V8_3V3; Bank voltage set on SOM 1.8V/3.3V;	SOC.W24
62		SD2_DATA0	0	Bank voltage set on SOM 1.8V/3.3V;	SOC.AB23
63		SD2_DATA1	0	Bank voltage set on SOM 1.8V/3.3V;	SOC.AB24
61		SD2_DATA2	0	Bank voltage set on SOM 1.8V/3.3V;	SOC.V24
65		SD2_DATA3	0	Bank voltage set on SOM 1.8V/3.3V;	SOC.V23
71		SD2_RESET_B	0	Alt function "SD2_RESET_B" can be used to control the SD card power in order to perform SD RESET function. Bank voltage set on SOM 1.8V/3.3V;	SOC.AB26
117		SD2_RESET_B	5		SOC.AG10

8.7.3. SD3 Signals

The uSDHC controller (SD3) is used internally for the eMMC or NAND interface on the SOM.

8.8. USB Ports

Two USB controllers and PHYs that support USB 2.0 interface are exposed on the VAR-SOM-MX8M-MINI connectors.
The USB 2.0 controller cores 0 and 1 are also named OTG1 and OTG2 Core respectively.

The following list provides features of each of the controller cores.

- High-Speed/Full-Speed/Low-Speed OTG core
- HS/FS/LS UTMI compliant interface connected to on-chip UTMI PHY
- High Speed, Full Speed and Low Speed operation in Host mode (with UTMI transceiver)
- High Speed, and Full Speed operation in Peripheral mode (with UTMI transceiver)
- Hardware support for OTG signaling, Session Request Protocol (SRP), Host Negotiation Protocol (HNP), and Attach Detection Protocol (ADP). ADP support includes dedicated timer hardware and register interface.
- Up to 8 bidirectional endpoints
- Core0(OTG1) Supports charger detection with register interface only
- Low-power mode with local and remote wake-up capability
- Embedded DMA controller in each core

8.8.1. USB Port1 Interface Signals

Table 18: USB2.0 Port 1 Interface signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
114		USB1_D_N	0	Differential Pair Negative side	SOC.A22
116		USB1_D_P	0	Differential Pair Positive side	SOC.B22
106		USB1_VBUS	0	USB PHY power pin; 5V tolerant	SOC.F22

8.8.2. USB Port2 Interface Signals

Table 19: USB2.0 Port 2 Interface signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
108		USB2_D_N	0	Differential Pair Negative side	SOC.A23
110		USB2_D_P	0	Differential Pair Positive side	SOC.B23
104		USB2_VBUS	0	USB PHY power pin; 5V tolerant	SOC.F23

8.8.3. USB OTG Interface Signals

Table below lists the available VAR-SOM-MX8M-MINI exposed pins, which can be optionally used to implement a complete OTG functions.

Table 20: USB Port 1 & 2 OTG Interface signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
94		USB1_ID	0	USB PHY ID pin; No GPIO function. USB OTG ID alternative signal location. "Low" means the SoC is Host role "High" means the SoC is Peripheral role.	SOC.D22
80		USB1_OTG_ID	1	Normally used as SD Card Detect for other SOM compatibility.	SOC.AD10
40		USB1_OTG_OC	1	USB OTG OC signal indicates that an overcurrent condition from an external current monitor on the downstream port occurred.	SOC.AD9
122		USB1_OTG_PWR	1	USB OTG PWR signal, active high control signal used to enable power to the downstream port	SOC.AB10
72		USB2_OTG_ID	1		SOC.AC10
91		USB2_OTG_OC	1	Optional interface for MCP2518; See section 8.16.1	SOC.AB9
99		USB2_OTG_PWR	1	Used internally with "TP" (RES-TOUCH_CS_B) Always exposed	SOC.AC9

8.9. PCIe

VAR-SOM-MX8M-MINI PCI exposes one PCI Express GEN 2 single lane interface. The PCI Express port requires an external 100MHz PCIe compliant reference clock if the function is enabled.

PCI port features:

- Dual mode (DM) controller provides a solution to implement a PCI Express port for a PCI Express root complex or endpoint application.
- Port solution includes the controller, an analog PHY macro, and application logic to source and sink data.
- PCI Express base specification 2.0 with maximum 5.0Gbps lane rate.
- Native PCIe PM Mechanisms

The PCIe controller implements the following standards:

- PCI Express Base Specification, Revision 4.0, Version 0.7
- PIPE Specification for PCI Express, Version 4.3, Intel Corporation
- PCI Local Bus Specification, Revision 3.0
- PCI Bus Power Management Specification, Revision 1.2
- PCI Express Card Electromechanical Specification, Revision 1.1

Note: Access to the above specification requires membership in PCI-SIG.

8.9.1. PCIE Signals

Table 21: PCIE Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
100		PCIE1_REF_CLK_N	0	Differential Pair Negative side PCIE compliant 100MHz reference clock; Terminate with 49.9 Ohm close to the connector.	SOC.A21
102		PCIE1_REF_CLK_P	0	Differential Pair Positive side PCIE compliant 100MHz reference clock; Terminate with 49.9 Ohm close to the connector.	SOC.B21
136		PCIE1_RX_N	0	Differential Pair Negative side	SOC.A19
134		PCIE1_RX_P	0	Differential Pair Positive side	SOC.B19
128		PCIE1_TX_N	0	Differential Pair Negative side	SOC.A20
130		PCIE1_TX_P	0	Differential Pair Positive side	SOC.B20

8.9.2. PCIE Side Band Signals

Table 22: PCIE Side band signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
83		PCIE1_CLKREQ_B	2	Used as debug UART on Variscite base board.	SOC.F19
174		PCIE1_CLKREQ_B	2		SOC.D13

8.10. Audio

The VAR-SOM-MX8M-MINI features analog and digital type of audio interfaces:

- WM8904 Audio codec Analog outputs & input interfaces:
  - Stereo line input
  - Stereo HP output
  - Digital microphone input
- **S**ynchronous **A**udio **I**nterface (SAI)
- **S**ony **P**hilips **D**igital **I**nter**F**ace (SPDIF)
- **P**ulse **D**ensity **M**odulation (PDM)

8.10.1. Analog Audio

Analog audio signals are part of the SOM WM8904 audio codec, available with **"AC" Configuration** only.

The Codec features stereo ground-referenced headphone amplifiers using the Wolfson 'Class-W' amplifier techniques -incorporating an innovative dual-mode charge pump architecture - to optimize efficiency and power consumption during playback. The ground-referenced headphone and line outputs eliminate AC coupling capacitors, and both outputs include common mode feedback paths to reject ground noise.

Figure 4 illustrates the connectivity for no large AC coupling capacitors

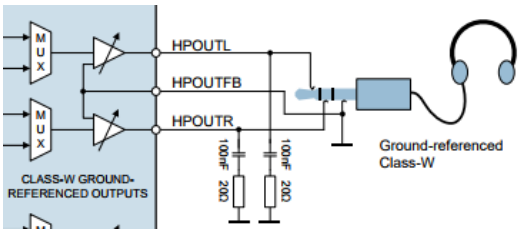


Figure 4: WM8904 Headphone connectivity

Refer to the official data sheet for detailed electrical characteristics of the relevant interfaces.

NOTE

The illustrated RC network is not included on SOMs under version V1.2;
Earlier SOM versions might exhibit high frequency noise.

Table 23: Analog Audio Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
196	AC	HPOUTFB		Signal source is Audio Codec. Headphone output ground loop noise rejection feedback	WM8904.14
198	AC	HPLOUT		Signal source is Audio Codec. Left headphone output (line or headphone output)	WM8904.13
200	AC	HPROUT		Signal source is Audio Codec. Right headphone output (line or headphone output)	WM8904.15
197	AC	LINEIN1_LP		Signal source is Audio Codec. Left channel input	WM8904.26
199	AC	LINEIN1_RP		Signal source is Audio Codec. Right channel input	WM8904.24
195		AGND		Audio Ground	AGND
18	AC	DMIC_CLK		Signal source is Audio Codec. Digital microphone clock output	WM8904.1
20	AC	DMIC_DATA		Signal source is Audio Codec. Digital microphone data input; Divided internally by 475 Ohm resistors to match Codec input levels.	WM8904.27

8.10.2. SAI - Synchronous Audio Interface

The I2S (or I2S) module of the i.MX 8M Mini SOC, provides a synchronous audio interface (SAI) that supports fullduplex serial interfaces with frame synchronization such as I2S, AC97, TDM, and codec/DSP interfaces.

Main Features of the SAI include:

- Transmitter with independent bit clock and frame sync supporting 8 data lines
- Receiver with independent bit clock and frame sync supporting 8 data lines
- Each data line can support a maximum Frame size of 32 words
- Word size of between 8-bits and 32-bits
- Word size configured separately for first word and remaining words in frame
- Asynchronous 8 x 32-bit FIFO for each transmit and receive data line
- Supports graceful restart after FIFO error
- Supports automatic restart after FIFO error without software intervention
- Supports packing of 8-bit and 16-bit data into each 32-bit FIFO word
- Supports combining multiple data line FIFOs into single data line FIFO
- Independent 32-bit timestamp counters and bit counters for monitoring transmit and
- receive progress

NOTE

Some of the features are not supported across all SAI instances; See i.MX 8M Mini Applications Processors Reference Manual for further details.

Besides the general audio input/output function, the audio interfaces will support the following features:

- SAI-1 supports up to 16-channels TX (8 lanes) and RX (8 lanes) at 384KHz/32-bit
- SAI-5 supports up to 8-channels TX (4 lanes) and RX (4 lanes) at 384KHz/32-bit
- SAI-2/3 supports up to 4-channels TX (2 lanes) and RX (2 lanes) at 384KHz/32-bit
- SAI-6 support up to 2-channels TX (1 lane) and RX (1 lane) at 384KHz/32-bit
- SAI-1 supports glue-less switching between PCM and DSD operation for popular audio DACs
- SAI-1 and SAI-5 supports up-to 8 channels of PDM
- SPDIF supports raw capture mode that can save all the incoming bits into audio buffer

The VAR-SOM-MX8M-MINI exposes all 5 SAI interfaces the i.MX 8M Mini SOC presents.

The SAI-1/2/3/5/6 and SPDIF-1 share GPIO pads on the chip through IOMUX. Common **U**se **C**ases (UC) supported by the audio interfaces are listed in the table below (many other configurations are possible). The number is the data lanes supported.

8.10.2.1. SAI Signals Definitions

The following table details the SAI interface signals definition.

Table 24: SAI interface signals definition

NAME	FUNCTION	DIR
SAI_TXC	Transmit Bit Clock. The bit clock is an input when externally generated and an output when internally generated.	I/O
SAI_TXFS	Transmit Frame Sync. The frame sync is an input sampled synchronously by the bit clock when externally generated and an output generated synchronously by the bit clock when internally generated.	I/O
SAI_TXD[0:0]	Transmit Data. The transmit data is generated synchronously by the bit clock and is tristate whenever not transmitting a word	O
SAI_RXC	Receive Bit Clock. The bit clock is an input when externally generated and an output when internally generated.	I/O
SAI_RXFS	Receive Frame Sync. The frame sync is an input sampled synchronously by the bit clock when externally generated and an output generated synchronously by the bit clock when internally generated.	I/O
SAI_RXD [0:0]	Receive Data. The receive data is sampled synchronously by the bit clock.	I
SAI_MCLK	Audio Master Clock.	I/O

8.10.2.2. SAI1 Signals

Table 25: SAI1 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
189	No TP	SAI1_MCLK	0	Exposed with no "TP" configuration	SOC.AB18
193	No TP	SAI1_RXC	0	Exposed with no "TP" configuration	SOC.AF16
148		SAI1_RXD0	0	Pull down 100K on SOM; Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AG15
84		SAI1_RXD1	0	Pull down 100K on SOM; Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AF15
187	No TP	SAI1_RXD2	0	Exposed with no "TP" configuration: Pull down 100K on SOM Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AG17
86		SAI1_RXD3	0	1K internal PD (not 100K for compatibility to other SOM) Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AF17
151		SAI1_RXD4	0	Pull down 100K on SOM; Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AG18
145		SAI1_RXD5	0	Pull down 100K on SOM; Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AF18
157		SAI1_RXD6	0	Pull down 100K on SOM; Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AG19
145		SAI1_RXFS	3	Pull down 100K on SOM; Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AF18
191	No TP	SAI1_RXFS	0	Exposed with no "TP" configuration	SOC.AG16
20	No AC	SAI1_TXC	1	With “AC” configuration do not alter PINMUX function.	SOC.AD15
177		SAI1_TXC	0		SOC.AC18
189	No TP	SAI1_TXC	2	Exposed with no "TP" configuration	SOC.AB18
147		SAI1_TXD0	0	Pull down 100K on SOM; Some NAND configuration include 10K pull up; Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AG20
196	No AC	SAI1_TXD0	1	With “AC” configuration do not alter PINMUX function.	SOC.AB15
148		SAI1_TXD1	2	Pull down 100K on SOM; Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AG15
152		SAI1_TXD1	0	Pull down 100K on SOM; Some NAND configuration include 10K pull up; Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AF20
197	No AC	SAI1_TXD1	1	With “AC” configuration do not alter PINMUX function.	SOC.AC15

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
141		SAI1_TXD2	0	Driven on SOM during POR_B; Some NAND configuration include 10K pull up; Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AG21
198	No AC	SAI1_TXD2	1	With “AC” configuration do not alter PINMUX function.	SOC.AD18
173		SAI1_TXD3	0	Driven on SOM during POR_B; Some NAND configuration include 10K pull down; Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AF21
199	No AC	SAI1_TXD3	1	With “AC” configuration do not alter PINMUX function.	SOC.AC14
200	No AC	SAI1_TXD4	1	With “AC” configuration do not alter PINMUX function.	SOC.AD13
18	No AC	SAI1_TXD5	1	With “AC” configuration do not alter PINMUX function.	SOC.AC13
155		SAI1_TXD5	0	Driven on SOM during POR_B; Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AF22
146		SAI1_TXD6	0	Pull down 100K on SOM; Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AG23
156		SAI1_TXD7	0	Pull down 100K on SOM; Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AF23
18	No AC	SAI1_TXFS	2	With “AC” configuration do not alter PINMUX function.	SOC.AC13
93		SAI1_TXFS	0		SOC.AB19
199	No AC	SAI1_TXFS	2	With “AC” configuration do not alter PINMUX function.	SOC.AC14
200	No AC	SAI1_TXFS	2	With “AC” configuration do not alter PINMUX function.	SOC.AD13

[1] For boot configuration refer to section 8.21

8.10.2.3. SAI2 Signals

Table 26: SAI2 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
73		SAI2_MCLK	0		SOC.AD19
22		SAI2_RXC	0		SOC.AB22
21		SAI2_RXD0	0		SOC.AC24
23		SAI2_RXD1	3		SOC.AC19
23		SAI2_RXFS	0		SOC.AC19
25		SAI2_TXC	0		SOC.AD22
26		SAI2_TXD0	0		SOC.AC22
24		SAI2_TXD1	3		SOC.AD23
24		SAI2_TXFS	0		SOC.AD23

8.10.2.4. SAI3 Signals

Table 27: SAI3 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
120		SAI3_MCLK	0		SOC.AD6
50		SAI3_RXC	0	Used internally with "WBD"; Function can be released if BT Buffer disabled. Always exposed;	SOC.AG7
51		SAI3_RXD	0	Used internally with "WBD"; Function can be released if BT Buffer disabled. Always exposed;	SOC.AF7
113		SAI3_RXD1	3		SOC.AG8
113		SAI3_RXFS	0		SOC.AG8
52		SAI3_TXC	0	Used internally with "WBD"; Function can be released if BT Buffer disabled. Always exposed;	SOC.AG6
82		SAI3_TXD	0		SOC.AF6
53		SAI3_TXD1	3	Used internally with "WBD"; Function can be released if BT Buffer disabled. Always exposed;	SOC.AC6
53		SAI3_TXFS	0	Used internally with "WBD"; Function can be released if BT Buffer disabled. Always exposed;	SOC.AC6

8.10.2.5. SAI5 Signals

Table 28: SAI5 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
20	No AC	SAI5_MCLK	0	With “AC” configuration do not alter PINMUX function.	SOC.AD15
73		SAI5_MCLK	1		SOC.AD19
120		SAI5_MCLK	2		SOC.AD6
189	No TP	SAI5_MCLK	1	Exposed with no "TP" configuration	SOC.AB18
50		SAI5_RXC	2	Used internally with "WBD"; Function can be released if BT Buffer disabled. Always exposed;	SOC.AG7
197	No AC	SAI5_RXC	0	With “AC” configuration do not alter PINMUX function.	SOC.AC15
51		SAI5_RXD0	2	Used internally with "WBD"; Function can be released if BT Buffer disabled. Always exposed;	SOC.AF7
148		SAI5_RXD0	1	Pull down 100K on SOM; Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AG15
198	No AC	SAI5_RXD0	0	With “AC” configuration do not alter PINMUX function.	SOC.AD18
53		SAI5_RXD1	2	Used internally with "WBD"; Function can be released if BT Buffer disabled. Always exposed;	SOC.AC6
84		SAI5_RXD1	1	Pull down 100K on SOM; Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AF15
199	No AC	SAI5_RXD1	0	With “AC” configuration do not alter PINMUX function.	SOC.AC14
52		SAI5_RXD2	2	Used internally with "WBD"; Function can be released if BT Buffer disabled. Always exposed;	SOC.AG6
187	No TP	SAI5_RXD2	1	Exposed with no "TP" configuration: Pull down 100K on SOM Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AG17
200	No AC	SAI5_RXD2	0	With “AC” configuration do not alter PINMUX function.	SOC.AD13
18	No AC	SAI5_RXD3	0	With “AC” configuration do not alter PINMUX function.	SOC.AC13
82		SAI5_RXD3	2		SOC.AF6
86		SAI5_RXD3	1	1K internal PD (not 100K for compatibility to other SOM) Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AF17
113		SAI5_RXFS	2		SOC.AG8
191	No TP	SAI5_RXFS	1	Exposed with no "TP" configuration	SOC.AG16
196	No AC	SAI5_RXFS	0	With “AC” configuration do not alter PINMUX function.	SOC.AB15
22		SAI5_TXC	1		SOC.AB22
177		SAI5_TXC	1		SOC.AC18

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
200	No AC	SAI5_TXC	3	With “AC” configuration do not alter PINMUX function.	SOC.AD13
18	No AC	SAI5_TXD0	3	With “AC” configuration do not alter PINMUX function.	SOC.AC13
21		SAI5_TXD0	1		SOC.AC24
147		SAI5_TXD0	1	Pull down 100K on SOM; Some NAND configuration include 10K pull up; Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AG20
23		SAI5_TXD1	2		SOC.AC19
24		SAI5_TXD1	1		SOC.AD23
152		SAI5_TXD1	1	Pull down 100K on SOM; Some NAND configuration include 10K pull up; Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AF20
25		SAI5_TXD2	1		SOC.AD22
141		SAI5_TXD2	1	Driven on SOM during POR_B; Some NAND configuration include 10K pull up; Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AG21
26		SAI5_TXD3	1		SOC.AC22
173		SAI5_TXD3	1	Driven on SOM during POR_B; Some NAND configuration include 10K pull down; Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AF21
23		SAI5_TXFS	1		SOC.AC19
93		SAI5_TXFS	1		SOC.AB19
199	No AC	SAI5_TXFS	3	With “AC” configuration do not alter PINMUX function.	SOC.AC14

[1] For boot configuration refer to section 8.21

8.10.2.6. SAI6 Signals

Table 29: SAI6 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
156		SAI6_MCLK	1	Pull down 100K on SOM; Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AF23
151		SAI6_RXC	2	Pull down 100K on SOM; Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AG18
145		SAI6_RXD0	2	Pull down 100K on SOM; Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AF18
155		SAI6_RXD0	1	Driven on SOM during POR_B; Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AF22
146		SAI6_RXFS	1	Pull down 100K on SOM; Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AG23
157		SAI6_RXFS	2	Pull down 100K on SOM; Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AG19
151		SAI6_TXC	1	Pull down 100K on SOM; Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AG18
145		SAI6_TXD0	1	Pull down 100K on SOM; Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AF18
155		SAI6_TXD0	2	Driven on SOM during POR_B; Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AF22
146		SAI6_TXFS	2	Pull down 100K on SOM; Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AG23
157		SAI6_TXFS	1	Pull down 100K on SOM; Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AG19

[1] For boot configuration refer to section 8.21

8.10.3. PDM - Microphone Interface (MICFIL)

The PDM module of the i.MX 8M Mini SOC, provides a popular way to deliver audio from microphones to the processor in several applications, such as mobile telephones.
Up to 8 channels can be implemented with 4 lanes.

PDM block main features are:
Fixed filtering characteristics for audio application.

- Full or partial set of channels operation with individual enable control.
- Programmable PDM clock generator.
- Programmable decimation rate.
- 16-bit signed output result.
- Overall stopband attenuation more than 80dB.
- Overall passband ripple less than 0.2dB.
- CIC filter
    - 5th order.
    - Programmable decimation rate.
- DC remover
    - First order IIR filter.
    - Programmable cut-off frequency.
- FIFOs with DMA capability.
    - Each FIFO is 8 entries length.
- Hardware Voice Activity Detector (HWVAD).
    - Interrupt capability.
    - Zero-Crossing Detection (ZCD) option.

The PDM Microphone Interface module is composed of:

- An input interface for each pair of PDM microphones.
- A decimation filter by channel.
- A FIFO by channel.
- A time generation unit.
- Shared interfaces to DMA, interrupts and SoC.
- One or more Hardware Voice Activity Detectors (HWVAD).

8.10.3.1. PDM Signals

Table 30: PDM Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
148		PDM_BIT0	3	Pull down 100K on SOM; Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AG15
198	No AC	PDM_BIT0	4	With “AC” configuration, do not alter PINMUX function.	SOC.AD18
84		PDM_BIT1	3	Pull down 100K on SOM; Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AF15
199	No AC	PDM_BIT1	4	With “AC” configuration, do not alter PINMUX function.	SOC.AC14
187	No TP	PDM_BIT2	3	Exposed with no "TP" configuration: Pull down 100K on SOM Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AG17
200	No AC	PDM_BIT2	4	With “AC” configuration, do not alter PINMUX function.	SOC.AD13
18	No AC	PDM_BIT3	4	With “AC” configuration, do not alter PINMUX function.	SOC.AC13
86		PDM_BIT3	3	1K internal PD (not 100K for compatibility to other SOM) Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AF17
156		PDM_CLK	3	Pull down 100K on SOM; Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AF23
189	No TP	PDM_CLK	3	Exposed with no "TP" configuration	SOC.AB18
197	No AC	PDM_CLK	4	With “AC” configuration, do not alter PINMUX function.	SOC.AC15

[1] For boot configuration refer to section 8.21

8.10.4. SPDIF – Sony Philips Digital Interface Format

A standard audio file transfer format, developed jointly by the Sony and Phillips corporations. It supports Transmitter and Receiver functionality including frequency measurement block that allows the precise measurement of an incoming sampling frequency.
The SPDIF receiver extracts the audio data from each SPDIF frame and places the data in the SPDIF Rx left and right FIFOs with Channel Status and User bits.
For the SPDIF transmitter, the audio data is provided by the processor dedicated registers along with Channel Status and User bits.

8.10.4.1. SPDIF Signals

Table 31: SPDIF Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
17		SPDIF_EXT_CLK	0		SOC.AF8
68		SPDIF_RX	0		SOC.AG9
69		SPDIF_TX	0		SOC.AF9

8.11. UART Interfaces

The VAR-SOM-MX8M-MINI exposes up to **four** UART interfaces some of which are multiplexed with other peripherals. UART2 is used on SOM for Bluetooth interface and can be accessible only if the on SOM buffer disabled or without ***"WBD" and "WB" Configuration***.

The UART includes the following features:

- High-speed TIA/EIA-232-F compatible, up to 4.15 Mbit/s
- Serial IR interface low-speed, IrDA-compatible (up to 115.2 Kbit/s)
- 9-bit or Multidrop mode (RS-485) support (automatic slave address detection)
- 7 or 8 data bits for RS-232 characters, or 9-bit RS-485 format
- 1 or 2 stop bits
- Programmable parity (even, odd, and no parity)
- Hardware flow control support for request to send (RTS_B) and clear to send (CTS_B) signals
- RS-485 driver direction control via CTS_B signal
- Edge-selectable RTS_B and edge-detect interrupts
- Transmitter FIFO empty interrupt suppression
- Can serve both as DTE or DCE device
- Auto baud rate detection (up to 115.2 Kbit/s)
- Receiver and transmitter enable/disable for power saving
- RX_DATA input and TX_DATA output can be inverted respectively in RS-232/RS-485 mode
- RTS_B, IrDA asynchronous wake (AIRINT), receive asynchronous wake (AWAKE) interrupts wake the processor from STOP mode

Table 32: UART I/O Configuration vs. mode

Port	DTE Mode		DCE Mode	
	Direction	Description	Direction	Description
UARTx_RTS_B	Output	UARTx_RTS_B from DTE to DCE	Input	UARTx_RTS_B from DTE to DCE
UARTx_CTS_B	Input	UARTx_CTS_B from DCE to DTE	Output	UARTx_CTS_B from DCE to DTE
UARTx_TX_ DATA	Input	Serial data from DCE to DTE	Output	Serial data from DCE to DTE
UARTx_RX _DATA	Output	Serial data from DTE to DCE	Input	Serial data from DTE to DCE

8.11.1.1. UART1 Signals

Table 33: UART1 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
24		UART1_CTS_B	4		SOC.AD23
55		UART1_CTS_B	1	Appear on pins 55 & 175 for other SOM modules UART compatibility	SOC.E18
21		UART1_RTS_B	4		SOC.AC24
57		UART1_RTS_B	1	Appear on pins 57 & 124 for other SOM modules UART compatibility	SOC.D18
124		UART1_RTS_B	1	Appear on pins 57 & 124 for other SOM modules UART compatibility	SOC.D18
22		UART1_RXD	4		SOC.AB22
54		UART1_RXD	0		SOC.E14
23		UART1_TXD	4		SOC.AC19
56		UART1_TXD	0		SOC.F13

8.11.1.2. UART2 Signals

Table 34: UART2 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
50		UART2_CTS_B	4	Used internally with "WBD"; Function can be released if BT Buffer disabled. Always exposed;	SOC.AG7
83		UART2_CTS_B	1	Used as debug UART on Variscite base board.	SOC.F19
51		UART2_RTS_B	4	Used internally with "WBD"; Function can be released if BT Buffer disabled. Always exposed;	SOC.AF7
85		UART2_RTS_B	1	Used as debug UART on Variscite base board.	SOC.F18
53		UART2_RXD	4	Used internally with "WBD"; Function can be released if BT Buffer disabled. Always exposed;	SOC.AC6
115		UART2_RXD	0		SOC.F15
52		UART2_TXD	4	Used internally with "WBD"; Function can be released if BT Buffer disabled. Always exposed;	SOC.AG6
171		UART2_TXD	0		SOC.E15

8.11.1.3. UART3 Signals

Table 35: UART3 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
41		UART3_CTS_B	1	Shared internally with "CN" or "TP" Always exposed	SOC.A7
39		UART3_RTS_B	1		SOC.B6
43		UART3_RXD	1	Shared internally with "CN" or "TP" Always exposed	SOC.D6
55		UART3_RXD	0	Appear on pins 55 & 175 for other SOM modules UART compatibility	SOC.E18
175		UART3_RXD	0	Appear on pins 55 & 175 for other SOM modules UART compatibility	SOC.E18
45		UART3_TXD	1	Shared internally with "CN" or "TP" Always exposed	SOC.B7
57		UART3_TXD	0	Appear on pins 57 & 124 for other SOM modules UART compatibility	SOC.D18
124		UART3_TXD	0	Appear on pins 57 & 124 for other SOM modules UART compatibility	SOC.D18

8.11.1.4. UART4 Signals

Table 36: UART4 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
77		UART4_CTS_B	1		SOC.A8
79		UART4_RTS_B	1		SOC.A6
75		UART4_RXD	1		SOC.E6
83		UART4_RXD	0	Used as debug UART on Variscite base board.	SOC.F19
70		UART4_TXD	1		SOC.B8
85		UART4_TXD	0	Used as debug UART on Variscite base board.	SOC.F18

8.12. ECSPI - Enhanced Configurable SPI

VAR-SOM-MX8M-MINI exposes all ECSPI1/ ECSPI2/ ECSPI3 pins.

The Enhanced Configurable Serial Peripheral Interface (ECSPI) is a full-duplex, synchronous, four-wire serial communication block with full-duplex enhanced Synchronous Serial Interface and data rate up to 52 Mbit/s.

Key features of the ECSPI include:

- Full-duplex synchronous serial interface
- Master/Slave configurable
- Four Chip Select (SS) signals to support multiple peripherals
- Transfer continuation function allows unlimited length data transfers
- 32-bit wide by 64-entry FIFO for both transmit and receive data
- Polarity and phase of the Chip Select (SS) and SPI Clock (SCLK) are configurable
- Direct Memory Access (DMA) support
- Refer to the product data sheet for the maximum operating frequency

8.12.1.1. ECSPI1 Signals

Table 37: ECSPI1 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
41		ECSPI1_MISO	0	Shared internally with "CN" or "TP" Always exposed	SOC.A7
45		ECSPI1_MOSI	0	Shared internally with "CN" or "TP" Always exposed	SOC.B7
43		ECSPI1_SCLK	0	Shared internally with "CN" or "TP" Always exposed	SOC.D6
39		ECSPI1_SS0	0		SOC.B6

8.12.1.2. ECSPI2 Signals

Table 38: ECSPI2 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
77		ECSPI2_MISO	0		SOC.A8
70		ECSPI2_MOSI	0		SOC.B8
75		ECSPI2_SCLK	0		SOC.E6
79		ECSPI2_SS0	0		SOC.A6

8.12.2. ECSPI3 Signals

Table 39: ECSPI3 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
115		ECSPI3_MISO	1		SOC.F15
56		ECSPI3_MOSI	1		SOC.F13
54		ECSPI3_SCLK	1		SOC.E14
171		ECSPI3_SS0	1		SOC.E15

8.13. QSPI/FlexSPI - Quad Serial Peripheral Interface

8.13.1. QSPI A & B Signals

QSPI A & B signals are used internally for the eMMC/NAND interface on the SOM and are not exposed to the connector.

8.14. NAND

The VAR-SOM-MX8M-MINI can be configured with NAND memory instead of an eMMC device.
All NAND signals are used internally and are not exposed to the connector.

8.15. I^2C

The VAR-SOM-MX8M-MINI SOM exposes up to three I2C interfaces on the connectors: I2C2, I2C3 and I2C4.

The Inter-Integrated Circuit (I2C) provides functionality of a standard I2C master and slave. I2C is a two-wire, bidirectional serial bus that provides a simple, efficient method of data exchange, minimizing the interconnection between devices.
This bus is suitable for applications requiring occasional communications over a short distance between many devices. The flexible I2C standard allows additional devices to be connected to the bus for expansion and system development.

The I2C has the following key features:

- Compatible with the I2C Bus Specification, version 2.1, by Philips Semiconductor (now NXP Semiconductors).
- Multi-master operation.
- After a reset, the I2C defaults to Slave Receive operations.
- Software programmability for one of 64 different serial clock frequencies:
    - Standard mode, I2C supports the data transfer rates up to 100 Kbits/s
    - In Fast mode, data transfer rates up to 400 Kbits/s can be achieved
- Software-selectable acknowledge bit
- Interrupt-driven, byte-by-byte data transfer
- Arbitration-lost interrupt with automatic mode switching from master to slave
- Calling address identification interrupt
- Start and stop signal generation/detection
- Repeated start signal generation
- Acknowledge bit generation/detection
- Bus-busy detection

8.15.1. I2C2 Signals

Table 40: I2C2 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
88		I2C2_SCL	0		SOC.D10
87		I2C2_SDA	0		SOC.D9

8.15.2. I2C3 Signals

Table 41: I2C3 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
92		I2C3_SCL	0	Used internally with "AC" (Codec I2C) - Do not alter pinmux! 10K internal PU included; Shared with Audio Codec	SOC.E10
90		I2C3_SDA	0	Used internally with "AC" (Codec I2C) - Do not alter pinmux! 10K internal PU included; Shared with Audio Codec	SOC.F10

8.15.3. I2C4 Signals

Table 42: I2C4 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
174		I2C4_SCL	0		SOC.D13
176		I2C4_SDA	0		SOC.E13

8.16. CAN

The VAR-SOM-MX8M-MINI SOM exposes one CAN-FD interface on the connector.

The Controller Area Network (CAN) module is a communication controller implementing the CAN protocol supporting both, CAN frames in the Classical format (CAN2.0B) and CAN Flexible Data Rate (CAN FD) format, as specified in ISO 11898-1:2015.

Protocol was primarily designed to be used as a vehicle serial data bus meeting the specific requirements of this field: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness and required bandwidth. The CAN module is a full implementation of the CAN protocol specification, which supports both standard and extended message frames.

8.16.1. CAN interface on SOM

As of SOM PCB version V1.3, changes include:

- CAN controller manufacturer PN used is MCP2518FD.
- Crystal modified from 20 MHz to 40 MHz.
- RX_INT connected to an unused GPIO : GPIO2_IO012
- TX_INT connected using resistor to pin 91 GPIO1_IO15

NOTE

Current MCP251x driver does not support TX_INT and this connection not implemented by SW.
Customers using CAN controller should leave pin 91 unconnected

8.16.2. CAN Signals

Table 43: CAN Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
46	CN	CAN_RX		Signal source is CAN FD controller.	MCP2518.2
44	CN	CAN_TX		Signal source is CAN FD controller.	MCP2518.1
91	CN	TX_INT		Optional interface for MCP2518; See section 8.16.1	MCP2518.9

8.17. Touch Panel

The VAR-SOM-MX8M-MINI SOM exposes one analogue touch panel controller interface.

TP Controller is responsible for providing control of ADC and touch screen analogue block to form a touch screen system, which achieves function of touch detection and touch location detection. The controller utilizes ADC hardware trigger function and control switches in touch screen analogue block. The controller supports 4-wire touch panel mode.

8.17.1. Touch Panel Signals

Table 44: Touch Panel Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
187	TP	TS_X-		Signal source is Resistive Touch controller.	TSC2046.8
189	TP	TS_X+		Signal source is Resistive Touch controller.	TSC2046.6
193	TP	TS_Y-		Signal source is Resistive Touch controller.	TSC2046.9
191	TP	TS_Y+		Signal source is Resistive Touch controller.	TSC2046.7

8.18. PWM - Pulse Width Modulation

The VAR-SOM-MX8M-MINI exposes all 4 of the PWM outputs.

The following features characterize the PWM:

- 16-bit up-counter with clock source selection
- Can be programmed to select one of three clock signals as its source frequency, with a maximum of 66MHz
- 4 x 16 FIFO to minimize interrupt overhead
- 12-bit pre-scaler for division of clock
- Sound and melody generation
- Active high or active low configured output
- Can be programmed to be active in low-power mode
- Can be programmed to be active in debug mode
- Interrupts at compare and rollover

8.18.1. PWM Signals

Table 45: PWM Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
17		PWM1_OUT	1		SOC.AF8
154		PWM1_OUT	1		SOC.AF14
176		PWM1_OUT	1		SOC.E13
40		PWM2_OUT	5	USB OTG OC signal indicates that an overcurrent condition from an external current monitor on the downstream port occurred.	SOC.AD9
68		PWM2_OUT	1		SOC.AG9
174		PWM2_OUT	1		SOC.D13
69		PWM3_OUT	1		SOC.AF9
90		PWM3_OUT	1	Used internally with "AC" (Codec I2C) - Do not alter pinmux! 10K internal PU included; Shared with Audio Codec	SOC.F10
99		PWM3_OUT	5	Used internally with "TP" (RES-TOUCH_CS_B) Always exposed	SOC.AC9
91		PWM4_OUT	5	Optional interface for MCP2518; See section 8.16.1	SOC.AB9
92		PWM4_OUT	1	Used internally with "AC" (Codec I2C) - Do not alter pinmux! 10K internal PU included; Shared with Audio Codec	SOC.E10
120		PWM4_OUT	1		SOC.AD6

8.19. GPT – General Purpose Timer

The VAR-SOM-MX8M-MINI exposes the GPT interface on its connectors.

Each GPT has a 32-bit up-counter. The timer counter value can be captured in a register using an event on an external pin. The capture trigger can be programmed to be a rising or/and falling edge. The GPT can also generate an event on the output compare pins and an interrupt when the timer reaches a programmed value. The GPT has a 12-bit pre-scaler, which provides a programmable clock frequency derived from multiple clock sources.

GPT Features include:

- One 32-bit up-counter with clock source selection, including external clock
- Two input capture channels with a programmable trigger edge
- Three outputs compare channels with a programmable output mode. A "forced compare" feature is also available
- Can be programmed to be active in low power and debug modes
- Interrupt generation at capture, compare, and rollover events
- Restart or free-run modes for counter operations

8.19.1. GPT Signals

Table 46: GPT Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
113		GPT1_CAPTURE1	1		SOC.AG8
53		GPT1_CAPTURE2	1	Used internally with "WBD"; Function can be released if BT Buffer disabled. Always exposed;	SOC.AC6
50		GPT1_CLK	1	Used internally with "WBD"; Function can be released if BT Buffer disabled. Always exposed;	SOC.AG7
51		GPT1_COMPARE1	1	Used internally with "WBD"; Function can be released if BT Buffer disabled. Always exposed;	SOC.AF7
52		GPT1_COMPARE2	1	Used internally with "WBD"; Function can be released if BT Buffer disabled. Always exposed;	SOC.AG6
82		GPT1_COMPARE3	1		SOC.AF6
92		GPT2_CLK	2	Used internally with "AC" (Codec I2C) - Do not alter pinmux! 10K internal PU included; Shared with Audio Codec	SOC.E10
90		GPT3_CLK	2	Used internally with "AC" (Codec I2C) - Do not alter pinmux! 10K internal PU included; Shared with Audio Codec	SOC.F10

8.20. Reference Clocks

Up to eight clock outputs from the CCM available from normal GPIO pads via IOMUX can be used to clock external devices.

8.20.1. Clock Signals

Table 47: Clock Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
99		CLKO1	6	Used internally with "TP" (RES-TOUCH_CS_B) Always exposed	SOC.AC9
91		CLKO2	6	Optional interface for MCP2518; See section 8.16.1	SOC.AB9
81		EXT_CLK1	6	Used internally with "CN" (CN-FD_CS_B) Always exposed	SOC.AG14
154		EXT_CLK2	6		SOC.AF14
96		EXT_CLK3	6		SOC.AG11
29		EXT_CLK4	6		SOC.AF11
154		REF_CLK_24M	5		SOC.AF14
81		REF_CLK_32K	5	Used internally with "CN" (CN-FD_CS_B) Always exposed	SOC.AG14

8.21. GPIO - General Purpose Input Output

The GPIO general-purpose input/output peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs.

- **When configured as an output:**
  It is possible to write to an internal register to control the state driven on the output pin
- **When configured as an input:**
  It is possible to detect the state of the input by reading the state of an internal register
- GPIO peripheral can produce CORE interrupts
- Input/output multiplexing controller (IOMUXC) to provide centralized pad control
- Up to 100 GPIO are available on the VAR-SOM-MX8M-MINI

8.21.1. GPIO Signals

The VAR-SOM-MX8M-MINI exposes up to 109 GPIO lines.

Table 48: GPIO Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
81		GPIO1_IO00	0	Used internally with "CN" (CN-FD_CS_B) Always exposed	SOC.AG14
154		GPIO1_IO01	0		SOC.AF14
48		GPIO1_IO02	0	Connected internally to PMIC WDOG_B input; Configured by default DTS to WDOG_B alternate function. PMIC behavior can be programmed to Cold or Warm or no reset. As WDOG_B alternate pin function could be used to initiate power up sequence in case of a watch dog event. E.g. "reboot" command To be used as GPIO; PMIC WDOG_B input should be programmed to No action.	SOC.AG13
150		GPIO1_IO03	0	Used internally with "TP" (RES-TOUCH_INT_B) Always exposed	SOC.AF13
153		GPIO1_IO05	0	Used internally with "CN" (CAN_INT_B) Always exposed	SOC.AF12
96		GPIO1_IO06	0		SOC.AG11
29		GPIO1_IO07	0		SOC.AF11
117		GPIO1_IO08	0		SOC.AG10
80		GPIO1_IO10	0	Normally used as SD Card Detect for other SOM compatibility.	SOC.AD10
72		GPIO1_IO11	0		SOC.AC10
122		GPIO1_IO12	0	USB OTG PWR signal, active high control signal used to enable power to the downstream port	SOC.AB10
40		GPIO1_IO13	0	USB OTG OC signal indicates that an overcurrent condition from an external current monitor on the downstream port occurred.	SOC.AD9
99		GPIO1_IO14	0	Used internally with "TP" (RES-TOUCH_CS_B) Always exposed	SOC.AC9

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
91		GPIO1_IO15	0	Optional interface for MCP2518; See section 8.16.1	SOC.AB9
74		GPIO1_IO16	5	Shared on SOM with "EC"; Powered by VDD_ENET. Do not alter pinmux with "EC" configuration	SOC.AC27
30		GPIO1_IO17	5	Shared on SOM with "EC"; Includes 1.5K Ohm PU to VDD_ENET; Do not alter pinmux with "EC" configuration	SOC.AB27
3	No EC	GPIO1_IO18	5	Powered by VDD_ENET pin RGMII Data out	SOC.AF25
5	No EC	GPIO1_IO19	5	Powered by VDD_ENET pin RGMII Data out	SOC.AG25
9	No EC	GPIO1_IO20	5	Powered by VDD_ENET pin RGMII Data out	SOC.AF26
11	No EC	GPIO1_IO21	5	Powered by VDD_ENET pin RGMII Data out	SOC.AG26
1	No EC	GPIO1_IO22	5	Powered by VDD_ENET pin; On some SOM modules this pin is GND; If placed in such carrier with no "EC" configuration define PAD as input! RGMII Transmit data Control	SOC.AF24
97	No EC	GPIO1_IO23	5	Powered by VDD_ENET pin; Includes series EMI filter ENET RGMII Transmit Clock: 125MHz @ 1000Mbps / 25MHz @ 100Mbps / 2.5MHz @ 10Mbps Samples TD [3:0] and TX_CTL	SOC.AG24
15	No EC	GPIO1_IO24	5	Powered by VDD_ENET pin RGMII Receive data Control	SOC.AF27
16	No EC	GPIO1_IO25	5	Powered by VDD_ENET pin; Includes series EMI filter ENET RGMII Receive Clock: 125MHz @ 1000Mbps / 25MHz @ 100Mbps / 2.5MHz @ 10Mbps Samples RD[3:0] and RX_CTL	SOC.AE26
4	No EC	GPIO1_IO26	5	Powered by VDD_ENET pin RGMII Data in	SOC.AE27
6	No EC	GPIO1_IO27	5	Powered by VDD_ENET pin RGMII Data in	SOC.AD27
10	No EC	GPIO1_IO28	5	Powered by VDD_ENET pin RGMII Data in	SOC.AD26
12	No EC	GPIO1_IO29	5	Powered by VDD_ENET pin RGMII Data in	SOC.AC26
60		GPIO2_IO13	5	Bank voltage set on SOM 1.8V/3.3V;	SOC.W23
64		GPIO2_IO14	5	Includes 2.4K PU on SOM to NVCC_SD2_1V8_3V3; Bank voltage set on SOM 1.8V/3.3V;	SOC.W24
62		GPIO2_IO15	5	Bank voltage set on SOM 1.8V/3.3V;	SOC.AB23
63		GPIO2_IO16	5	Bank voltage set on SOM 1.8V/3.3V;	SOC.AB24
61		GPIO2_IO17	5	Bank voltage set on SOM 1.8V/3.3V;	SOC.V24
65		GPIO2_IO18	5	Bank voltage set on SOM 1.8V/3.3V;	SOC.V23

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
71		GPIO2_IO19	5	Alt function "SD2_RESET_B" can be used to control the SD card power in order to perform SD RESET function. Bank voltage set on SOM 1.8V/3.3V;	SOC.AB26
196	No AC	GPIO3_IO19	5	With “AC” configuration do not alter PINMUX function.	SOC.AB15
197	No AC	GPIO3_IO20	5	With “AC” configuration do not alter PINMUX function.	SOC.AC15
198	No AC	GPIO3_IO21	5	With “AC” configuration do not alter PINMUX function.	SOC.AD18
199	No AC	GPIO3_IO22	5	With “AC” configuration do not alter PINMUX function.	SOC.AC14
200	No AC	GPIO3_IO23	5	With “AC” configuration do not alter PINMUX function.	SOC.AD13
18	No AC	GPIO3_IO24	5	With “AC” configuration do not alter PINMUX function.	SOC.AC13
20	No AC	GPIO3_IO25	5	With “AC” configuration do not alter PINMUX function.	SOC.AD15
191	No TP	GPIO4_IO00	5	Exposed with no "TP" configuration	SOC.AG16
148		GPIO4_IO02	5	Pull down 100K on SOM; Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AG15
84		GPIO4_IO03	5	Pull down 100K on SOM; Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AF15
187	No TP	GPIO4_IO04	5	Exposed with no "TP" configuration: Pull down 100K on SOM Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AG17
86		GPIO4_IO05	5	1K internal PD (not 100K for compatibility to other SOM) Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AF17
151		GPIO4_IO06	5	Pull down 100K on SOM; Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AG18
145		GPIO4_IO07	5	Pull down 100K on SOM; Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AF18
157		GPIO4_IO08	5	Pull down 100K on SOM; Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AG19
93		GPIO4_IO10	5		SOC.AB19
177		GPIO4_IO11	5		SOC.AC18
147		GPIO4_IO12	5	Pull down 100K on SOM; Some NAND configuration include 10K pull up; Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AG20

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
152		GPIO4_IO13	5	Pull down 100K on SOM; Some NAND configuration include 10K pull up; Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AF20
141		GPIO4_IO14	5	Driven on SOM during POR_B; Some NAND configuration include 10K pull up; Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AG21
173		GPIO4_IO15	5	Driven on SOM during POR_B; Some NAND configuration include 10K pull down; Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AF21
155		GPIO4_IO17	5	Driven on SOM during POR_B; Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AF22
146		GPIO4_IO18	5	Pull down 100K on SOM; Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AG23
156		GPIO4_IO19	5	Pull down 100K on SOM; Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AF23
189	No TP	GPIO4_IO20	5	Exposed with no "TP" configuration	SOC.AB18
23		GPIO4_IO21	5		SOC.AC19
22		GPIO4_IO22	5		SOC.AB22
21		GPIO4_IO23	5		SOC.AC24
24		GPIO4_IO24	5		SOC.AD23
25		GPIO4_IO25	5		SOC.AD22
26		GPIO4_IO26	5		SOC.AC22
73		GPIO4_IO27	5		SOC.AD19
113		GPIO4_IO28	5		SOC.AG8
50		GPIO4_IO29	5	Used internally with "WBD"; Function can be released if BT Buffer disabled. Always exposed;	SOC.AG7
51		GPIO4_IO30	5	Used internally with "WBD"; Function can be released if BT Buffer disabled. Always exposed;	SOC.AF7
53		GPIO4_IO31	5	Used internally with "WBD"; Function can be released if BT Buffer disabled. Always exposed;	SOC.AC6
52		GPIO5_IO00	5	Used internally with "WBD"; Function can be released if BT Buffer disabled. Always exposed;	SOC.AG6
82		GPIO5_IO01	5		SOC.AF6
120		GPIO5_IO02	5		SOC.AD6
69		GPIO5_IO03	5		SOC.AF9
68		GPIO5_IO04	5		SOC.AG9
17		GPIO5_IO05	5		SOC.AF8
43		GPIO5_IO06	5	Shared internally with "CN" or "TP" Always exposed	SOC.D6

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
45		GPIO5_IO07	5	Shared internally with "CN" or "TP" Always exposed	SOC.B7
41		GPIO5_IO08	5	Shared internally with "CN" or "TP" Always exposed	SOC.A7
39		GPIO5_IO09	5		SOC.B6
75		GPIO5_IO10	5		SOC.E6
70		GPIO5_IO11	5		SOC.B8
77		GPIO5_IO12	5		SOC.A8
79		GPIO5_IO13	5		SOC.A6
88		GPIO5_IO16	5		SOC.D10
87		GPIO5_IO17	5		SOC.D9
92		GPIO5_IO18	5	Used internally with "AC" (Codec I2C) - Do not alter pinmux! 10K internal PU included; Shared with Audio Codec	SOC.E10
90		GPIO5_IO19	5	Used internally with "AC" (Codec I2C) - Do not alter pinmux! 10K internal PU included; Shared with Audio Codec	SOC.F10
174		GPIO5_IO20	5		SOC.D13
176		GPIO5_IO21	5		SOC.E13
54		GPIO5_IO22	5		SOC.E14
56		GPIO5_IO23	5		SOC.F13
115		GPIO5_IO24	5		SOC.F15
171		GPIO5_IO25	5		SOC.E15
55		GPIO5_IO26	5	Appear on pins 55 & 175 for other SOM modules UART compatibility	SOC.E18
57		GPIO5_IO27	5	Appear on pins 57 & 124 for other SOM modules UART compatibility	SOC.D18
124		GPIO5_IO27	5	Appear on pins 57 & 124 for other SOM modules UART compatibility	SOC.D18
83		GPIO5_IO28	5	Used as debug UART on Variscite base board.	SOC.F19
85		GPIO5_IO29	5	Used as debug UART on Variscite base board.	SOC.F18

8.22. JTAG

The System JTAG Controller (SJC) provides debug and test control with maximum security. The test access port (TAP) is designed to support features compatible with the IEEE standard 1149.1 v2001 (JTAG). Support IEEE P1149.6 extensions to the JTAG standard are for AC testing of selected IO signals.

The JTAG port allows debug-related control and status, such as putting selected cores into reset and/or debug mode and the ability to monitor individual core status signals via JTAG. JTAG port interfaces the M4 and Cortex A53 Cores DAP - debug access port.
The VAR-SOM-MX8M-MINI JTAG MOD pin is hardware tied low and enables the Daisy chain ALL mode only, used for common SW debug (High speed and production).

VAR-SOM-MX8M-MINI exposes JTAG signals on a header (not assembled by default) on the SOM top left side.

8.22.1. JTAG Header Signals & Location

Table 49: JTAG Header Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
1		JTAG_VREF		Connected to SOM_3V3_PER via 150 Ohm	
2		JTAG_TMS			SOC.F27
3		GND			
4		JTAG_TCK		Include PD of 8.2K Ohm	SOC.F26
5		GND			
6		JTAG_TDO			SOC.E26
7		GND		Via 0 Ohm resistor on SOM	
8		JTAG_TDI			SOC.E27
9		JTAG_TRST_B		Active low signal;	SOC.C27
10		POR_B			

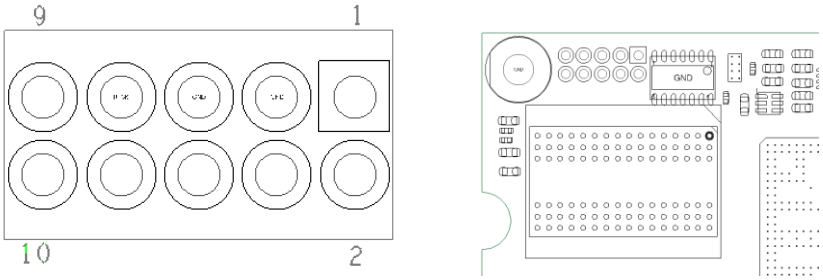


Figure 5: JTAG Header location and pin numbering.

8.23. General System Control

8.23.1. Boot Configuration

The VAR-SOM-MX8M-MINI can be programmed to boot from the following sources:

- Internal source (depends on the orderable configuration):
  - eMMC Flash memory
  - NAND Memory **(Currently not released, 256/512MB will be supported!)**
- External source:
  - SD Card

The selection of the boot device is implemented by logic on SOM which drives the BOOT_CFG lines. Pin 42 of the connector used to control boot device.

ATTENTION

External drivers connected to BOOT_CFG lines exposed to the connector should be disabled on during reset (POR_B) + 30ms, otherwise they may change the boot option and the SOM will not boot.

8.23.2. Boot Configuration Signals

Table 50: Boot Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
148		BOOT_CFG00	6	Pull down 100K on SOM; Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AG15
84		BOOT_CFG01	6	Pull down 100K on SOM; Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AF15
187	No TP	BOOT_CFG02	6	Exposed with no "TP" configuration: Pull down 100K on SOM Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AG17
86		BOOT_CFG03	6	1K internal PD (not 100K for compatibility to other SOM) Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AF17
151		BOOT_CFG04	6	Pull down 100K on SOM; Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AG18
145		BOOT_CFG05	6	Pull down 100K on SOM; Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AF18
157		BOOT_CFG06	6	Pull down 100K on SOM; Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AG19
147		BOOT_CFG08	6	Pull down 100K on SOM; Some NAND configuration include 10K pull up; Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AG20

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
152		BOOT_CFG09	6	Pull down 100K on SOM; Some NAND configuration include 10K pull up; Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AF20
141		BOOT_CFG10	6	Driven on SOM during POR_B; Some NAND configuration include 10K pull up; Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AG21
173		BOOT_CFG11	6	Driven on SOM during POR_B; Some NAND configuration include 10K pull down; Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AF21
155		BOOT_CFG13	6	Driven on SOM during POR_B; Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AF22
146		BOOT_CFG14	6	Pull down 100K on SOM; Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AG23
156		BOOT_CFG15	6	Pull down 100K on SOM; Part of boot config; Do not drive until after SOM_3V3_PER rise + 30ms	SOC.AF23
42		BOOT_SEL		Controls internal OR external boot source; Include 100K pull up to NVCC_SNVS_1V8; Connected via diode for 3.3V compatibility 0 =EXT. BOOT 1/Float=INT. BOOT	Internal Boot Logic input

NOTE

BOOT_CFG[0..15] should not be driven only after SOM_3V3_PER rise + 30ms
External Source: refers to device connected to SD2 pins e.g. SD card; see section SD2 Signals
Internal Source: Refers to the device configured as SOM storage: eMMC or NAND

8.23.3. General System Control Signals

The user must ensure not to drive any pins/function of the SOM before the appropriate IO domain power is up.

SOM_3V3_PER output is used to power most of the SOM pins and could be used to control the custom board power. Refer to Symphony-Board schematics for implementation suggestion. Table *51* details the SOM system control signals and *Figure 6* for timing diagram.

NOTE

General control signals: ONOFF, PMIC_ON_REQ, PMIC_STBY_REQ are internally powered by NVCC_SNVS_1V8; added circuitry on SOM cause them to be 3.3V compatible;

Table 51: System Control Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
143		ONOFF	0	**SOC input** with internal 100K PU to VCC_SOM **In OFF mode:** brief connection to GND causes the internal power management state machine to change state to ON. **In ON mode**: brief connection to GND generates an interrupt (intended to initiate a software-controllable power-down). **To Force OFF**: approximate 5 second or more connection to GND Not used leave Floating	SOC.A25
142		PMIC_ON_REQ	0	**SOC output**; Reflects the PMIC state; Can be used for custom board power control. Note: Buffered on SOM from internal signal; VCC_SOM level; Can be used to control the custom board power.	SOC.A24
98		PMIC_PWRON_B		**PMIC input** to control SOM power rails; PWRON_B is an active-low input for triggering the system to reset. On 1st power up will cause cold reset on SOM; After 1st power up, PMIC can be programmed to Cold or Warm or no reset on input event; This input is triggered by High to Low + Low > 10ms and cannot be used to hold the SOC boot up process; Users requiring the SOM not to boot once power applied required to hold VCC_SOM down.	PMIC.40
140		PMIC_STBY_REQ	0	**SOC output** which controls the PMIC state; Note: Buffered on SOM from internal signal; VCC_SOM level; Transition 0 to 1: Enter Standby Transition 1 to 0: Wake up from standby Can be used to control custom board power for standby state;	SOC.E24
48		WDOG_B	1	**SOC output**: Connected internally to **PMIC WDOG_B input**; Configured by default DTS to WDOG_B alternate function. PMIC behavior can be programmed to Cold or Warm or no reset; default Cold reset; As WDOG_B alternate pin function could be used to initiate power up sequence in case of a watch dog event, e.g. "reboot" command To use as GPIO; PMIC behavior for PMIC WDOG_B input should be programmed to No reset.	SOC.AG13

[1] Once the **WDOG** is activated, it must be serviced by the software on a periodic basis. If servicing does not take place, the timer times out. Upon timeout, the WDOG asserts the internal system reset signal, WDOG_RESET_B to the System Reset Controller (SRC). There is also a provision for WDOG signal assertion by timeout counter expiration. There is an option of programmable interrupt generation before the counter actually times out. The time at which the interrupt needs to be generated prior to counter timeout is programmable. There is a power down counter which is enabled out of any reset (POR, Warm/Cold). This counter has a fixed timeout period of 16 seconds, upon which it asserts the WDOG signal.
WDOG runs at 3.3V as part of the GPIO1 bank.

8.23.3.1. Power Up Sequence

Figure 6 illustrates the timing relationship between VCC_SOM and SOM_3V3_PER to the internal (not exposed) POR_B and boot configuration pins drive;
Delay measured on the Symphony Board which includes a power up reset circuitry.

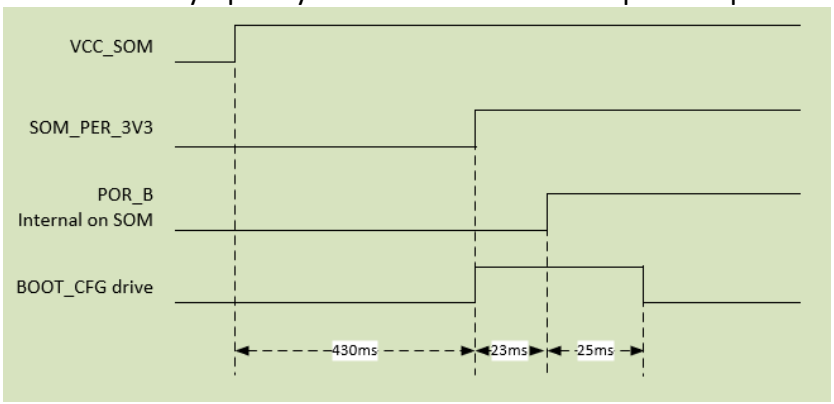


Figure 6 : VAR-SOM-MX8M-MINI power up timing

Figure 7 illustrates cold reset following PMIC_PWRON_B going low for >10ms debounce time.

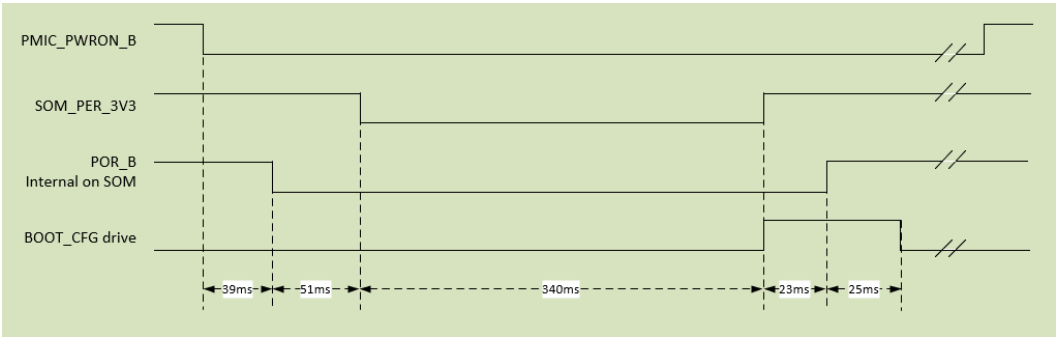


Figure 7 : VAR-SOM-MX8M-MINI Cold Reset Timing

8.24. Power

8.24.1. Power

Table 52: Power Pins

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
49		SOM_3V3_PER		Power output from SOM; Rises with last power rail; Can be used to control base board power and reset circuitry. Max. 100mA draw allowed;	
106		USB1_VBUS	0	USB PHY power pin; 5V tolerant	SOC.F22
104		USB2_VBUS	0	USB PHY power pin; 5V tolerant	SOC.F23
32		VCC_SOM		SOM Power	VCC_SOM
34		VCC_SOM		SOM Power	VCC_SOM
36		VCC_SOM		SOM Power	VCC_SOM
103		VCC_SOM		SOM Power	VCC_SOM
105		VCC_SOM		SOM Power	VCC_SOM
107		VCC_SOM		SOM Power	VCC_SOM
109		VCC_SOM		SOM Power	VCC_SOM
111		VCC_SOM		SOM Power	VCC_SOM
38	No EC	VDD_ENET	0	ENET pins group power IN **"EC" configuration:** * Not Connected **No "EC" configuration:** Must supply one option (Max. 50mA required) - * RMII uses 1.8 or 3.3V. * RGMII uses 1.8 or 2.5V. * GPIO 1.8V/2.5V/3.3V	SOC.W22

NOTE

Users using SOM_3V3_PER as a supply power source, required to add 10uF to 20uF ceramic capacitor rated to > 6.3V.

8.24.2. Ground

Table 53: Ground Pins

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
2		GND		Digital Ground	
7		GND		Digital Ground	
8		GND		Digital Ground	
13		GND		Digital Ground	
14		GND		Digital Ground	
19		GND		Digital Ground	
27		GND		Digital Ground	
28		GND		Digital Ground	
37		GND		Digital Ground	
47		GND		Digital Ground	
58		GND		Digital Ground	
59		GND		Digital Ground	
66		GND		Digital Ground	
67		GND		Digital Ground	
76		GND		Digital Ground	
78		GND		Digital Ground	
89		GND		Digital Ground	
95		GND		Digital Ground	
101		GND		Digital Ground	
112		GND		Digital Ground	
118		GND		Digital Ground	
126		GND		Digital Ground	
132		GND		Digital Ground	
138		GND		Digital Ground	
139		GND		Digital Ground	
144		GND		Digital Ground	
149		GND		Digital Ground	
158		GND		Digital Ground	
159		GND		Digital Ground	
169		GND		Digital Ground	
172		GND		Digital Ground	
178		GND		Digital Ground	
179		GND		Digital Ground	
185		GND		Digital Ground	
195		AGND		Audio Ground	

8.24.3. Not Connected Pins

Table 54: NC Pins

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
1	EC	NC		With “EC” configuration this pin in Not Connected.	
31		NC		High power modules VCC_SOM Other GND Current SOM Not connect for compatibility	
33		NC		High power modules VCC_SOM Other GND Current SOM Not connect for compatibility	
35		NC		High power modules VCC_SOM Other GND Current SOM Not connect for compatibility	
38	EC	NC		With “EC” configuration this pin in Not Connected.	
44	No CN	NC		Pin not connected with No “CN” configuration!	
46	No CN	NC		Pin not connected with No “CN” configuration!	
97	EC	NC		With “EC” configuration this pin in Not Connected.	
180	No LD	NC		Pin not connected with No “LD” configuration!	
181	No LD	NC		Pin not connected with No “LD” configuration!	
182	No LD	NC		Pin not connected with No “LD” configuration!	
183	No LD	NC		Pin not connected with No “LD” configuration!	
184	No LD	NC		Pin not connected with No “LD” configuration!	
186	No LD	NC		Pin not connected with No “LD” configuration!	
188	No LD	NC		Pin not connected with No “LD” configuration!	
190	No LD	NC		Pin not connected with No “LD” configuration!	
192	No LD	NC		Pin not connected with No “LD” configuration!	
194	No LD	NC		Pin not connected with No “LD” configuration!	

9. Electrical Specifications

9.1. Absolute Maximum Ratings

Table 55: Absolute Maximum Ratings

Parameter	Min	Max	Unit
VCC_SOM	-0.3	3.6	V
USB_VBUS	-0.3	5.25	V

9.2. Operating Conditions

Table 56: Operating Ranges

Parameter	Min.	Typ.	Max.	Unit
VCC_SOM	3.25	3.35	3.45	V
USB_VBUS	2.5	5	5.25	V

Important NOTE

VCC_SOM must rise above 3.35V for >200us to ensure proper power up sequence; After power-up VCC_SOM can go down to the minimum value;

9.3. Power Consumption

Table 57: VAR-SOM-MX8M-MINI Power Consumption

Mode	Voltage	Current	Power	Conditions
Run	3.35V	0.680A	2.28W	Linux up, Wi-Fi connected and Iperf is running 802.11 ac 5GHz **(Dual Band Module)**
Run	3.35V	0.585A	1.96W	Linux up, Wi-Fi connected and Iperf is running 802.11 n 2.4GHz **(Dual Band Module**)
Run	3.35V	0.570A	1.91W	Linux up, Wi-Fi connected and Iperf is running 802.11 n 2.4GHz **(Single Band Module**)
Run	3.35V	0.364A	1.22W	Linux up
VFHD video playback	3.35V	0.424A	1.42W	On 800x480 LCD
Standby	3.4V	15mA	51mW	Memory in retention mode [1]
Off (RTC)	3.35V	300uA	1mW	All power rails are Off, only Internal SoC RTC is powered

[1] NOTE: Tested with IT module grade having total of 2GB DRAM

9.4. Peripheral Voltage Levels

Most of the peripheral interface lines used as inputs or output to the VAR-SOM-MX8M-MINI uses 3.3V LVCMOS levels, except the following interfaces: PCIe, USB, MIPI-DSI, MIPI-CSI, LVDS, SD2, ENET, MDIO/MDC

***PCIe/USB/MIPI-DSI/MIPI-CSI/LVDS*:** Interfaces follow a different standard since they are high-speed signals.

SD2: (SDIO lines) interface IOs will change voltage between 3.3V and 1.8V depending on the SD card capabilities.
With other alternative function user can determine the voltage SD2 IOs bank will be 1.8V or 3.3V;

ENET: interface available in case SOM is ordered **without "EC"** configuration. IOs will run according to the power fed to VDD_ENET (pin 38) (1.8V/2.5V/3.3V).

MDIO/MDC:
MDIO, MDC signals (pins 30, 74 respectively) are referenced to VDD_ENET rail.
In case a SOM is ordered **with "EC"** Configuration, VDD_ENET is produced internally on SOM and is set to 1.8V or 2.5V depending on the SOM revision:
In SOM revisions up to v1.4 - VDD_ENET is set 2.5V
In SOM revisions v1.5 and higher - VDD_ENET is set 1.8V

In case a SOM is ordered **without "EC"** configuration. IOs will run according to the power fed to VDD_ENET (pin 38) (1.8V/2.5V/3.3V).

10. Environmental Specifications

Table 58: Environmental Specifications

Parameter	Min	Max
Commercial Operating Temperature Range	0°C	70°C
Extended Operating Temperature Range	0°C	85°C
Industrial Operating Temperature Range	-40°C	85°C
Storage temperature	-40°C	85°C
Relative humidity (operation)	10%	90%
Relative humidity (storage)	05%	95%
Prediction Method Model: Telcordia Technologies Special Report SR-332, Issue 4 50°C, GB	> 5737 Khrs	

NOTE

Extended and industrial temperature ranges based only on the operating temperature grade of the SOM components. Customer should consider specific thermal design for the final product based upon the specific environmental and operational conditions.

11. Mechanical Drawings

11.1. Carrier Board Mounting

The SOM has two holes which are plated holes and connected to GND, for securing it to the carrier board.

11.2. Standoffs

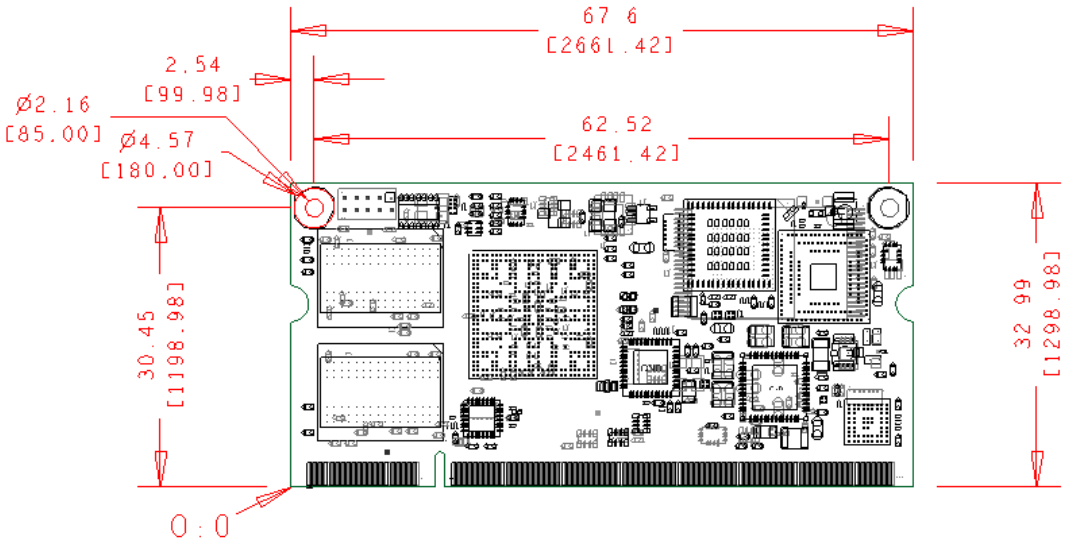
Customers requiring a mechanical solution for mounting in harsh vibration environments can use the following standoff:

Manufacturer: **MAC8**

PN: **TH-1.6-2.5-M2-B**

11.3. SOM Dimensions

Figure 8 illustrates the top view of the VAR-SOM-MX8M-MINI size and mounting holes relative location. **All dimensions given in millimeter[mils] units**.



UNITS: Milimeters [Mils]

Figure 8: VAR-SOM-MX8M-MINI Top View Mechanics

11.3.1. CAD Files

CAD files are available for download at http://www.variscite.com/

12. Legal Notice

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Variscite warrants performance of its products to the specifications in effect at the date of shipment. Variscite reserves the right to make changes to its products and specifications or to discontinue any product or service without notice. Customers should therefore obtain the latest version of relevant product information from Variscite to verify that their reference is current.

Testing and other quality control techniques are utilized to the extent that Variscite deems necessary to support its warranty.

Specific testing of all parameters of each device is not necessarily performed unless required by law or regulation.

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