Symphony-Board

Variscite

CONTENT

Disclaimer:

Schematics are for reference only.
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Schematics are subject to change without notice.

Revision History

Document	Carrier	
1.0	1.0	Initial
1.1	1.1	Released
1.2	1.1	Updated Block Diagrams Added SH1 wire short symbol Updated Compatability value for SOM pins 68,69,176 Updated SOM pin 22 net name Fixed U22.B1, C113.1 net name Fixed R1-R2,R35-R38 net name
1.3	1.2	Removed SH1 wire short, J1.68 routed to capacitive touch Changed R29 to C185 Changed R123,R127 to N.C. Added resistors R130-132 Removed ADC_INxx alternate function from VAR-SOM-MX8 Symbol Updated PCIe resistor assembly note
1.4	1.2	Updated Parallel Camera/HDMI/DP Note Fixed ETH pin names VAR-SOM-MX8X Symbol
1.5	1.2A	Disconnected R129
1.6	1.2A	Added VAR-SOM-MX8M-MINI Block Diagram and Symbol PRE-RELEASE VERSION !!!!! Subject to change without notice
1.7	1.2B	Fixed VAR-SOM-MX8M-MINI Symbol Changed U29,U30,U31 to P/N: FPF2193 Changed R60 to 47K
1.8	1.2C	Update VAR-SOM-MX8M-MINI Symbol to V1.1 with side notes for v1.0B(Early access customers) Update VAR-SOM-MX8M-MINI Block Diagram POR circuitry fed by VCC_SOM: see U7 R60 R61 R40 R60 D5 Removed
1.9	1.2D	Raise VCC_3V3 to Nominal 3.39V for VAR-SOM-MX8M-MINI/NANO power up threshold voltage requirement of >3.35V
1.10	1.2E	Reference for new designs: (changes not implemented in V1.2 BRD) * Added x2 studs for heat plate support * Base_per_3v3 added slew rate limit * U7 (Base POR circuit) added CB_WDOG resistor assmbly options * U29 U30 U31 - Added assembly note * VAR-SOM-MX8M-NANO pages added with symbol pinout * VAR-SOM-MX6 Connector update - added NC on /*/ assembly options * Power switch in OFF position discharge of Custom rails added * Ethernet magnetics - support two Manf: Pulse & UDE; * Base RJ45 LEDs matched to SOM behaviour;
1.11	1.3	* Added VAR-SOM-MX8M-PLUS Preliminary Symbol and Block Diagram Symbol is Pre-Release Version! Subject to change without notice! * All C1210 capacitor footprint updated to C1210_v0 * MS1 to MS6 not assembled
1.12	1.3A	* ETH1 PHY clock filter U9 replaced with 49.9 Ohm /0603 resistor * Added design note for ETH1 switches U8 and U10.
1.13	1.4	* MS5 and MS6 location adopted to heatplate design - Layout * Update J1 Manufacturer PN, NAME and footprint to epresent the assembled part * Replace PCIe AC caps on RX lines with 0 ohm resistors * Updated VAR-SOM-MX8M-PLUS Symbol pins 1 58 80, swap pins 41 43 and 84 147 * J19 Modify Camera connector orientation * Remove U8 U10 analog switches on ETH1 * U9 revert to EMI filter on RGMII_RX clock line * Added RN1 RN2 RN3 R151 R136 isolating stubs on ETH1 RGMII signals * U26 footprint updated to DS * Y1 C68 C67 updated * Support for VAR-SOM-6UL boot: - BOOT_MODE1 - R117 assembled - BOOT_MODE0 - Added PD R149 - USB#A PWR to HOST J23 always enabled * Remove R39 on pin J1.156 to support SOM-MX8MP 2nd MIPI-CSI Lane2 routing * J3 J30 pinout change
1.14	1.4A	* Support for VAR-SOM-MX8MP USB OTG - Changed U5.P4 Pull for board identification, U21.9 connected to GPIO: - Changed R43,R130,R106 to N.C. - Changed R44,R132 to Assembled * Changed Q4 P/N from: TPS27082L (EOL) to -> TPS27081A * Updated VAR-SOM-MX8M-PLUS Block Diagram, Symbol pins 36,38 names * Added notes for SOM pins 29,79,84
1.15	1.4A	Changes in v1.14/1.4A for R43,R44 were not implemented (part of board identification) and only appear in revision history; board identification implemented via EEPROM U3. Board identification required for OS to identifiy method of OTG ID used: PTN5150 or GPIO
1.16	1.5	* Modified VCC_3V3 to 3.35V nominal for all SOMs. For VAR-SOM-MX8M-MINI/NANO, power up threshold voltage requirement of >3.35V is implemented using Q10,R152 * Added note for VAR-SOM-MX8M-MINI/NANO pin 91
1.17	1.5	* Updated note for I2C#B pull up resistors
1.18	1.5	* Updated note for PTN36043BXY chip
1.19	1.5A	* Q10 changed to 2N7002P,215 Transistor Q10 changed to 2N7002P to stabilize the SOM voltage in the OFF state. Old transisitor leakage current (IDG) changed the feedback current and increased the SOM voltage. 2N7002P does not have SG diode that allowed IDSS to flow into the Gate * SOM Pin 84 Note changed
1.20	1.6	Ethernet PHY replaced to ADIN1300 R22,R23,R35,R36 assembled with Ferrite Bead C185 assembled with 10K resistor, R30 not assembled U2 changed to CBTL02043B USB3 crossover switch changed to CBTL02043B
1.21	1.6A	Due to EOL: U35 changed to NFL18ZT207H1A3D Due to allocation problems: U13 changed to SN65HVD232QDR
1.22	1.6B	Due to allocation problems: U22,U29,U30,U31 changed to P/N: FPF2194
1.23	1.6C	Added VAR-SOM-AM62 Block Diagram and Symbol Added VAR-SOM-MX93 Block Diagram and Symbol Temporary removed compatibility notes Added hand wired EXP_MDIO_EN line.

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File: 00. Cover

Size	Document Number	Rev
Custom	Symphony-Board	1.6C_R1.2

Project	
Symphony-Board	

Designer:	Relief Int.	Approved By:
Date:	Monday, January 30, 2023	Sheet 1 of 24

VPC1
PCB
VPC3404-2U

03.SOM

For cross probing between SOM symbol and the specific SOM Connector used, set the "Implementation" property value in SOM port symbol to one of the following:

1. VAR-SOM-MX6
2. VAR-SOM-MX8
3. VAR-SOM-MX8X
4. VAR-SOM-MX8M-MINI
5. VAR-SOM-MX8M-NANO
6. VAR-SOM-MX8M-PLUS
7. VAR-SOM-MX93
8. VAR-SOM-AM62

For complete alternate function per pin and specific SOM: please refer to "VAR-SOMs_Compatibility_and_Pinout.XLS " located at: ftp://ftp.variscite.com/SOM_Compatibility

OFF PAGE CONNECTOR INDEX:
1. Function# :Interface common to ALL SOMs
2. J1.xxx-Function :Interface common to certains SOMs or Used for carrier board common function
3. J1.xxx :No common interface

Compatability list
Describes the ALT per SOM for compatibility.
Order of names: (MX6/MX8/MX8X/MX8MM/MX8MN/MX8MP)
Note: single name means identical name for all.

Implementation = VAR-SOM-MX93

SOM_3V3
Output from SOM
Used to enable base peripherals power

R57:
SOM-MX8X:
Remove for conneting LICELL

SOM-MX8M-PLUS :
With no "EC" remove & supply power for ENET0 IOs

R55:
SOM-MX6/MX8:
Remove for connecting 1588

VAR-SOM-6UL BOOT

SOM-MX8M-PLUS:
Pin 84 is routed via on SOM buffer with 10K pull up

SOM-MX8M-PLUS:
Pin 79 is routed via on SOM buffer with 10K pull up

R18:
SOM-MX6/MX8I:
Remove for connecting 1588

TP8:
SOM-MX6/MX8/MX8X:
TAMPER IOs Interface

In VAR-SOM-MX93 SOM pin 29 EXP_INT is referenced to 1.8V. There is a 12K pull down resistor on the SOM to divide the voltage on this pin.
In VAR-SOM-MX8 SOM pin 29 EXP_INT is referenced to 1.8V.
When using pin 29 as an input pin driven by higher input voltage, use an external voltage divider or limit the current using a series resistor to a maximum of 1mA.

R8 R10 R12 R13:
MX8X SOM:
without Touch screen controller on SOM, remove to prevent stubs on High speed lines

MECHANICS

HEATPLATE SUPPORT STANDOFF

MS5 TH-1.6-2.5-M2
MS6 TH-1.6-2.5-M2
Variscite_PN = VCN0262

SOM MOUNTING STANDOFF

MS1 TH-1.6-2.5-M2
MS2 TH-1.6-2.5-M2
MS3 TH-1.6-2.5-M2
MS4 TH-1.6-2.5-M2

SymphonyBoard STANDOFF

NC HOLE3 NC HOLE1 NC HOLE4 NC HOLE2

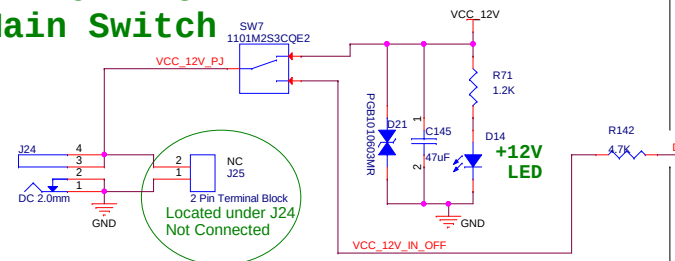
Fiducial

FID1 FID2 FID3 FID4 NC NC NC NC

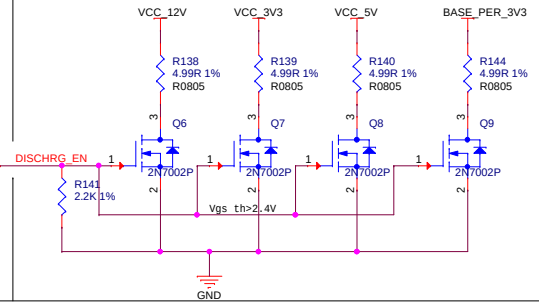
Title: 03. SOM			
Size: A2	Document Number: Symphony-Board	Project: Symphony-Board	Rev: 1.6C_R1.23
Designer: Aviad H.		Approved By:	
Date: Tuesday, January 31, 2023		Sheet 2 of 24	

05. Power,Reset,Boot,RTC,EEPROM

12VDC INPUT
Main Switch



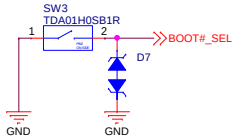
POWER DISCHARGE



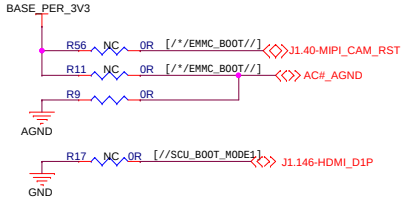
SOM BOOTSTRP

Boot Options:
OFF : INT
ON : SD

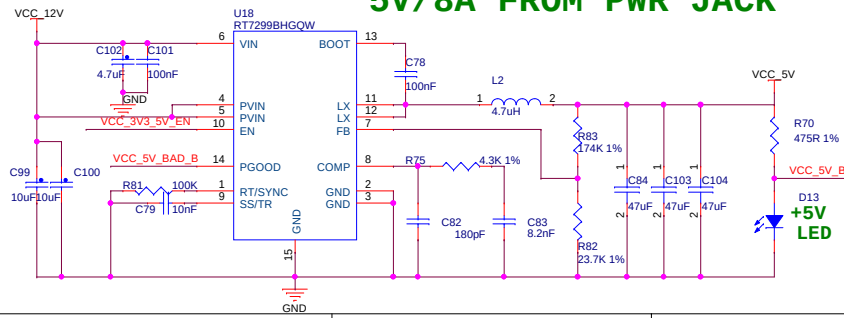
Internal boot is from eMMC
MX6 for eMMC boot see additional changes note



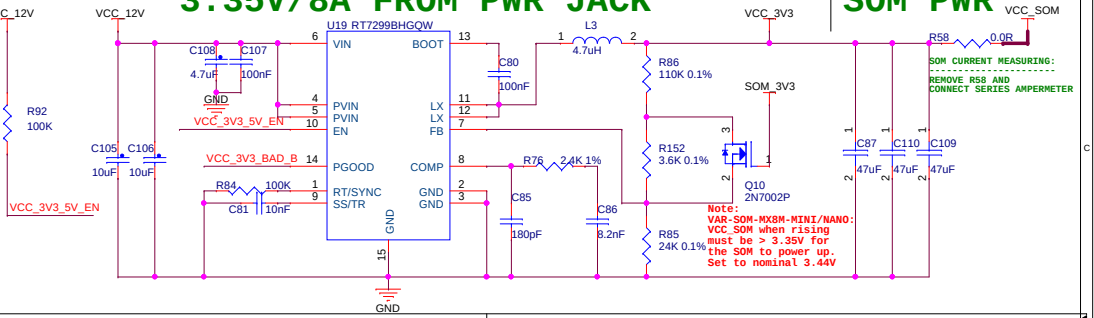
For supporting MX6 eMMC boot option:
Remove R9
Assemble R56,R11
Note: Normal configuration is with NAND



5V/8A FROM PWR JACK

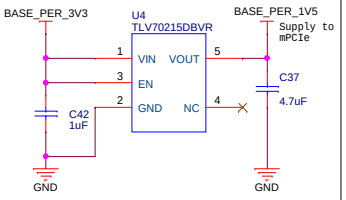


3.35V/8A FROM PWR JACK

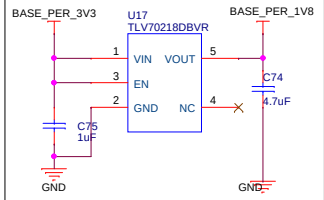


SOM PWR

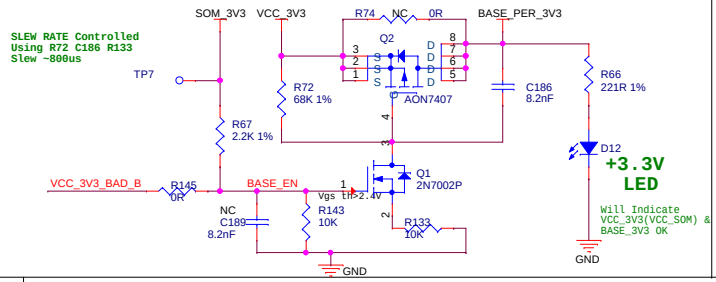
1.5V BASE



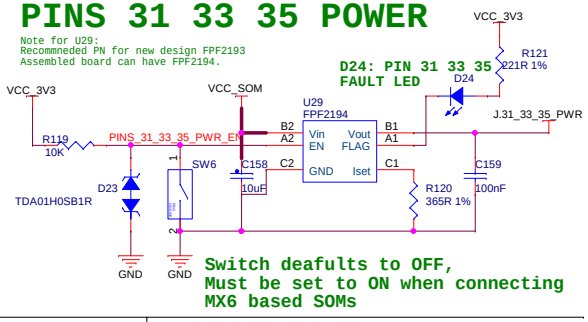
1.8V BASE



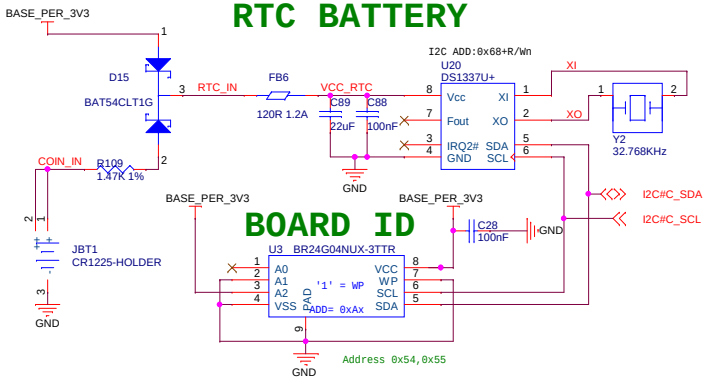
BASE_3V3



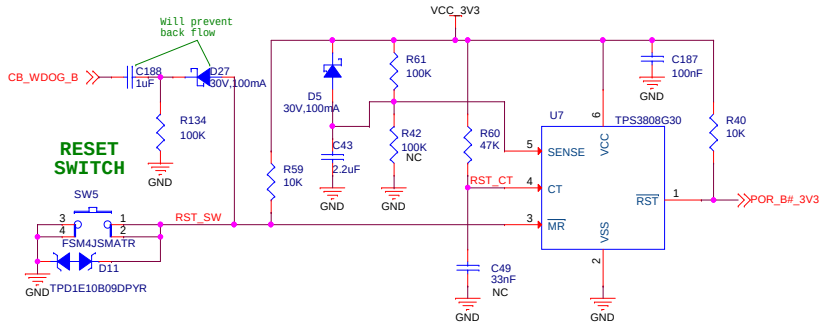
PINS 31 33 35 POWER



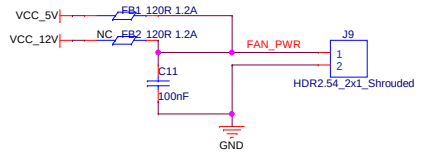
RTC BATTERY



RESET CIRCUITRY



FAN PWR



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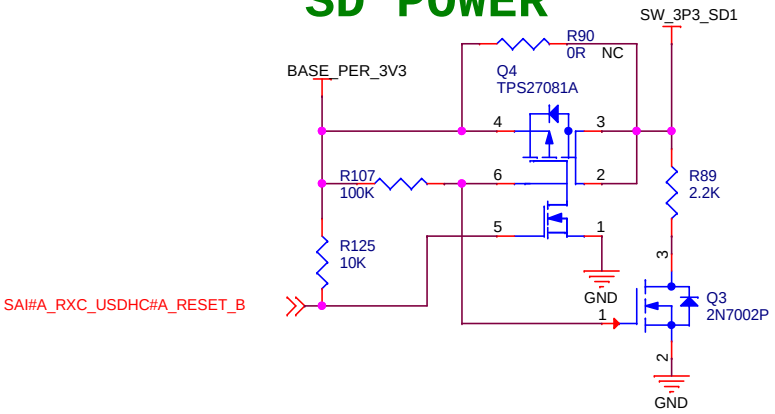
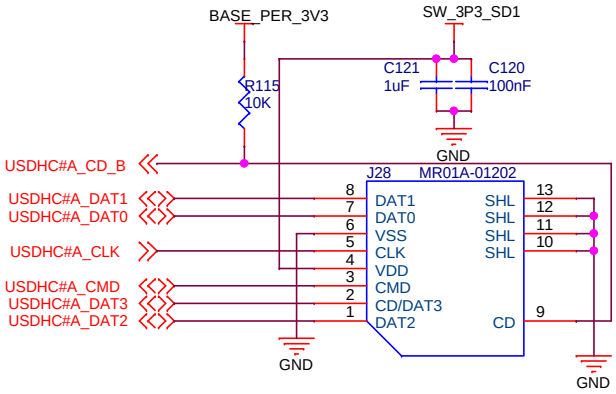
Title: 05. Power,Reset,Boot,RTC,EEPROM			
Size: A3	Document Number	Project	Rev: 1.6C_R1.23
Designer: Aviad H.		Approved By:	
Date: Monday, January 30, 2023		Sheet 3 of 24	

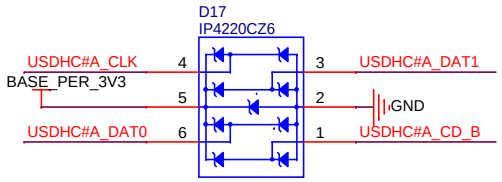
06. uSD, Audio,CAN

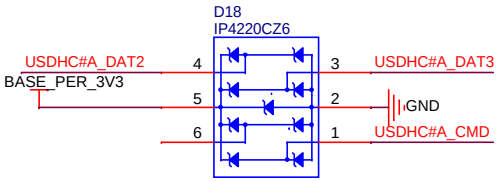
SD POWER



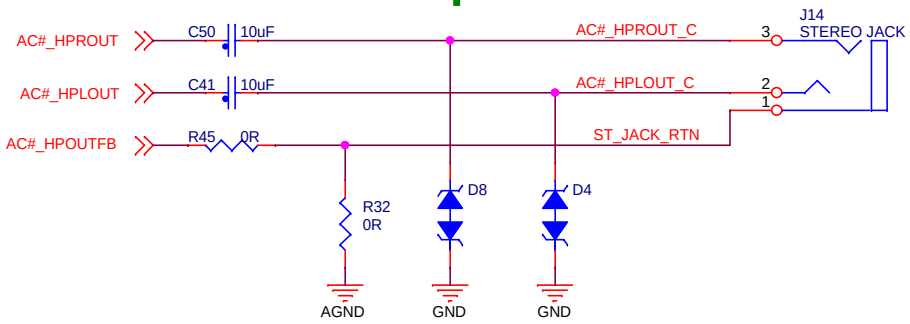
uSD CARD



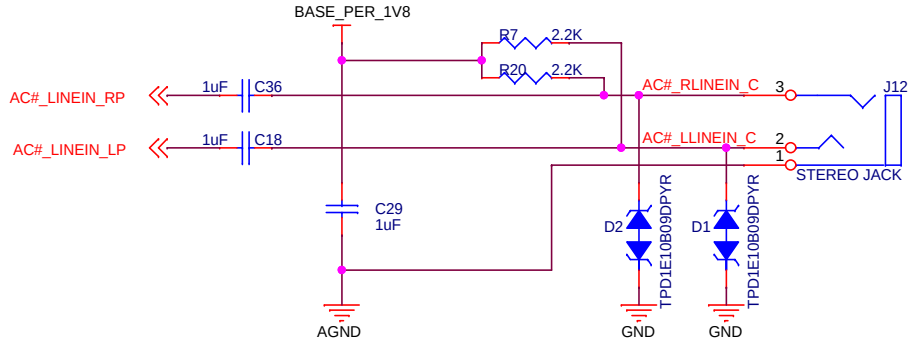




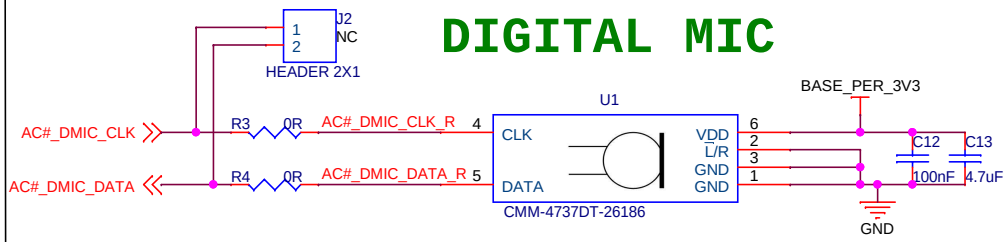
Headphones



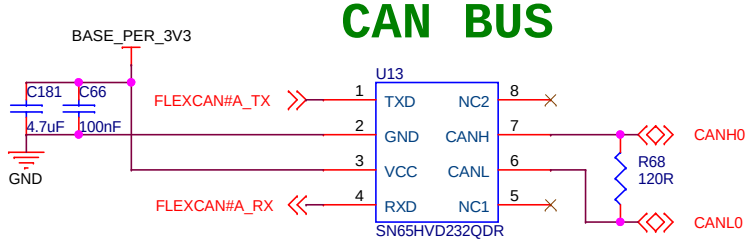
Line In



DIGITAL MIC



CAN BUS



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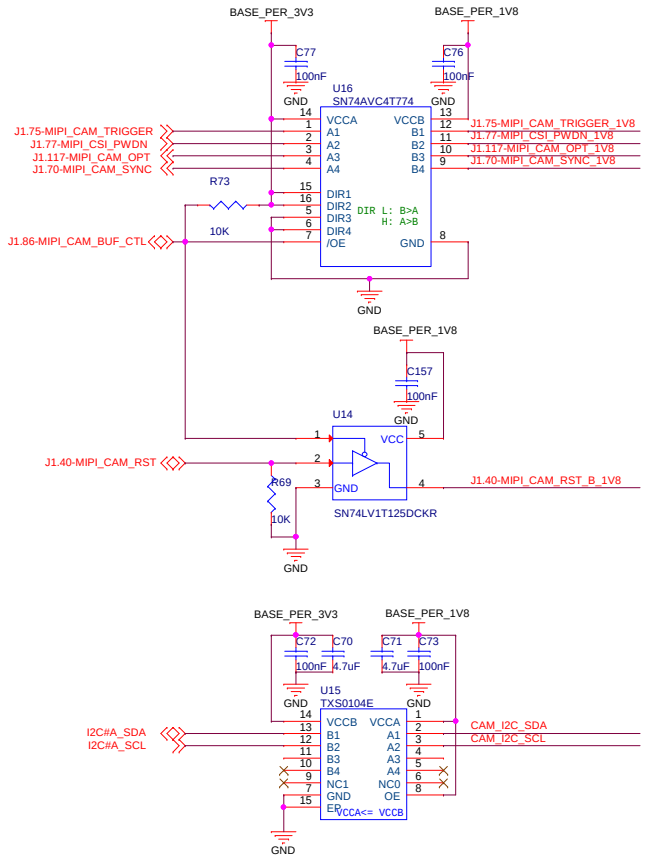
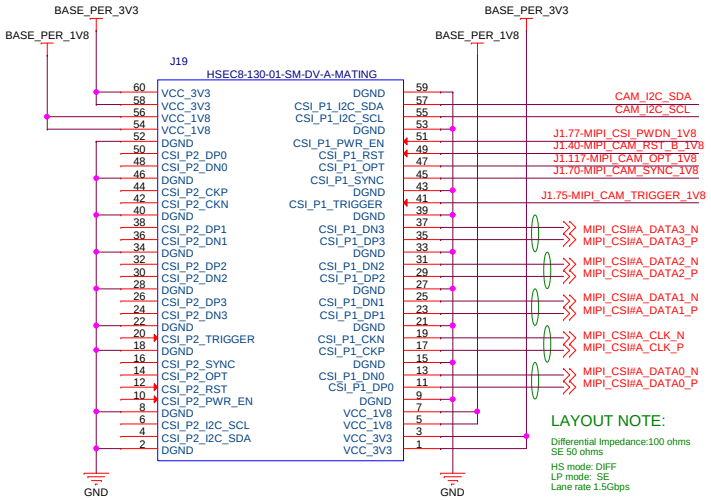
Title: 06. uSD, Audio,CAN			
Size: A4	Document Number: Symphony-Board	Project: Symphony-Board	Rev: 1.6C_R1.2
Designer: Aviad H.		Approved By:	
Date: Monday, January 30, 2023		Sheet 4 of 24	

07. Camera, HDMI, DP



MIPI-CSI



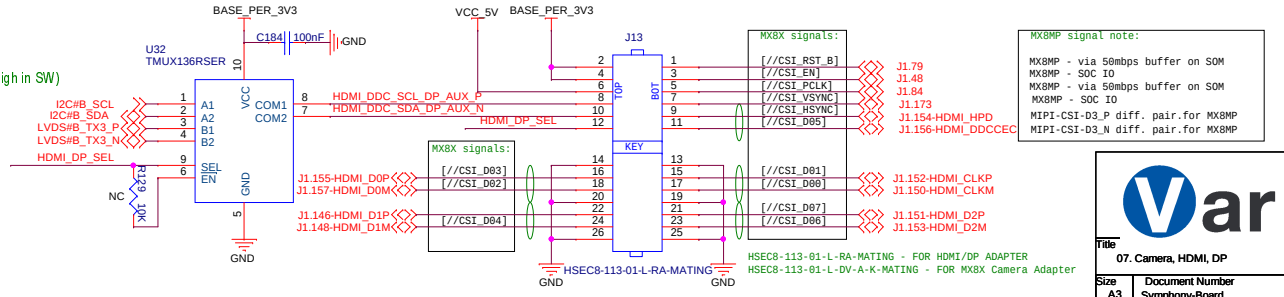
Note:
MIPI_CSI#A signals appears on bottom side of J19 as of SymphonyBoard V1.4.

J13: MX6/MX8-HDMI, MX8-DP, MX8X-CSI, MX8MP-2nd MIPI-CSI

Note for U32 (analog switch):
Switch is to enable support for the following adapters:
Parallel camera, HDMI, DisplayPoty and second MIPI-CSI .

Switch select controlled on adaptor will select between:
1) I2C#B which can export
VAR-SOM-MX8X: I2C3 Used by parallel camera
VAR-SOM-MX8: HDMI DDC Used by HDMI (GPIO1_22 in should be set High in SW)
2) LVDS#B_TX3 which can export:
VAR-SOM-MX8(DP assembly option): HDMI AUX used by DP

Switch can be omitted when designing for only one of the the above interfaces.



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Title: 07. Camera, HDMI, DP			
Size: A3	Document Number: Symphony-Board	Project: Symphony-Board	Rev: 1.6C_R1.23
Designer: Aviad H.		Approved By:	
Date: Monday, January 30, 2023		Sheet 5 of 24	

08. Ethernet

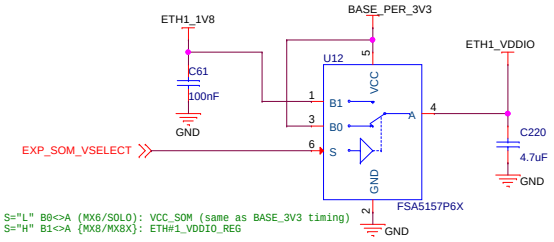
Header/Stub isolation resistors

J1.54-ENET1_RGMII_RXD3	ENET1_RGMII_RXD3	NC	R173	0R	J1.54_EXT
J1.71-ENET1_RGMII_RXD2	ENET1_RGMII_RXD2	NC	R174	0R	J1.71_EXT
J1.122-ENET1_RGMII_RXD0	ENET1_RGMII_RXD0	NC	R175	0R	J1.122_EXT
J1.81-ENET1_RGMII_RXD1	ENET1_RGMII_RXD1	NC	R176	0R	J1.81_EXT
J1.120-ENET1_RGMII_RX_CTL	ENET1_RGMII_RX_CTL	NC	49.9R 1%	R151	J1.120_EXT
J1.57-ENET1_RGMII_RXC	ENET1_RGMII_RXC				
	ENET1_RGMII_RXC_AR	NC	1.0K 1%	R136	J1.57_EXT
J1.113-ENET1_RGMII_TX_CTL	ENET1_RGMII_TX_CTL	NC	R179	0R	J1.113_EXT
J1.96-ENET1_RGMII_TXC	ENET1_RGMII_TXC	NC	R180	0R	J1.96_EXT
J1.73-ENET1_RGMII_TXD0	ENET1_RGMII_TXD0	NC	R181	0R	J1.73_EXT
J1.177-ENET1_RGMII_TXD1	ENET1_RGMII_TXD1	NC	R182	0R	J1.177_EXT
J1.56-ENET1_RGMII_TXD2	ENET1_RGMII_TXD2	NC	R177	0R	J1.56_EXT
J1.55-ENET1_RGMII_TXD3	ENET1_RGMII_TXD3	NC	R178	0R	J1.55_EXT

Note:
Customer requiring usage of J30 header (located on bottom side) should assemble these resistors if not assembled by default

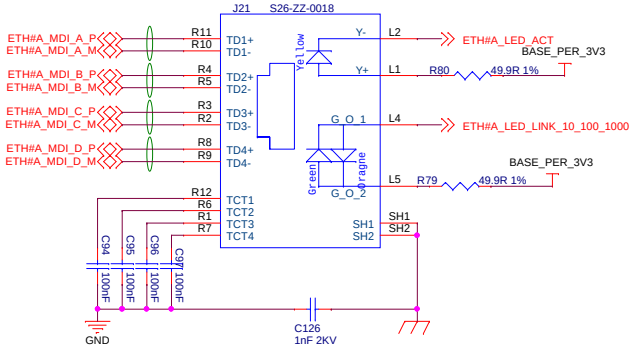
VDD_ENET for SOM-MX8/MX8X/MX8MP

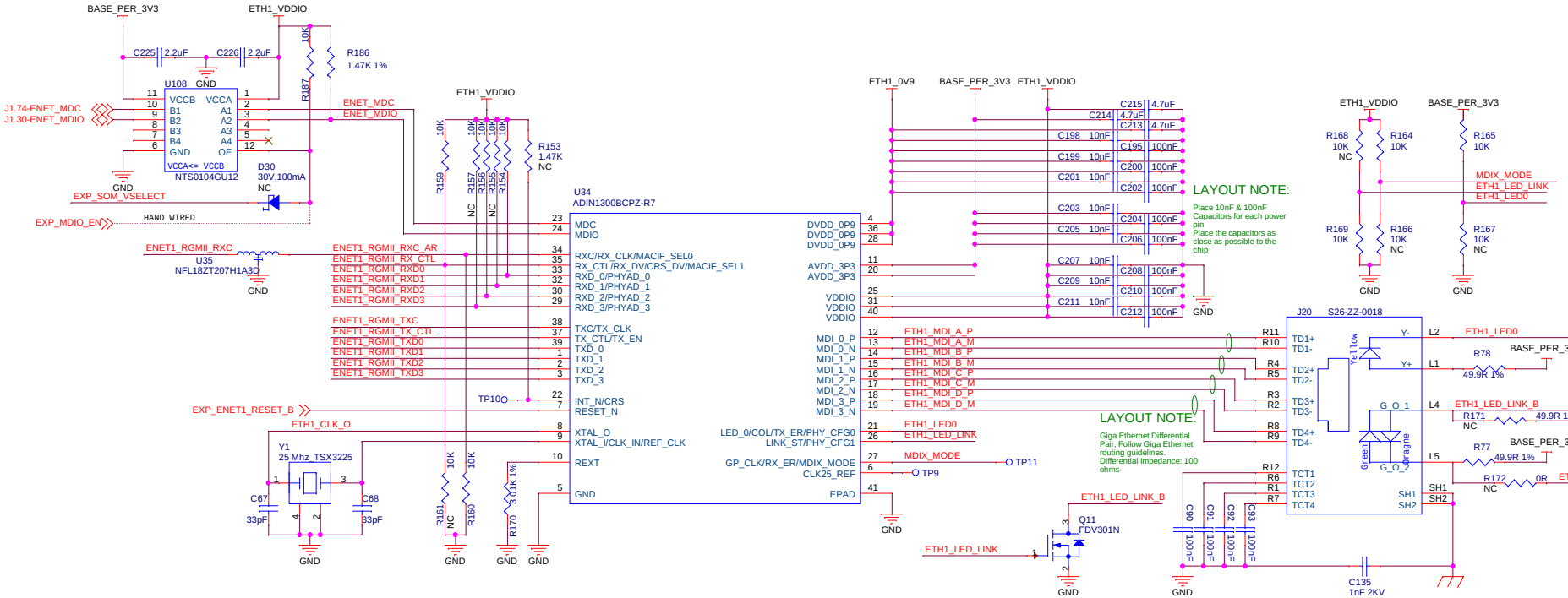
Power for ENET1_RGMII IOs on SOM power fed from pin J1.38
For specific SOM listed above, requiring second ETH port on ENET1 this power should be set to 1.8V source from U11 PHY

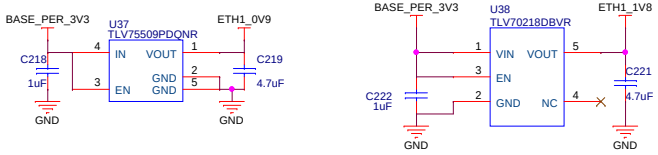


Gigabit Ethernet (Internal)

LAYOUT NOTE: Giga Ethernet Differential Pair, Follow Giga Ethernet routing guidelines. Differential Impedance: 100 ohms





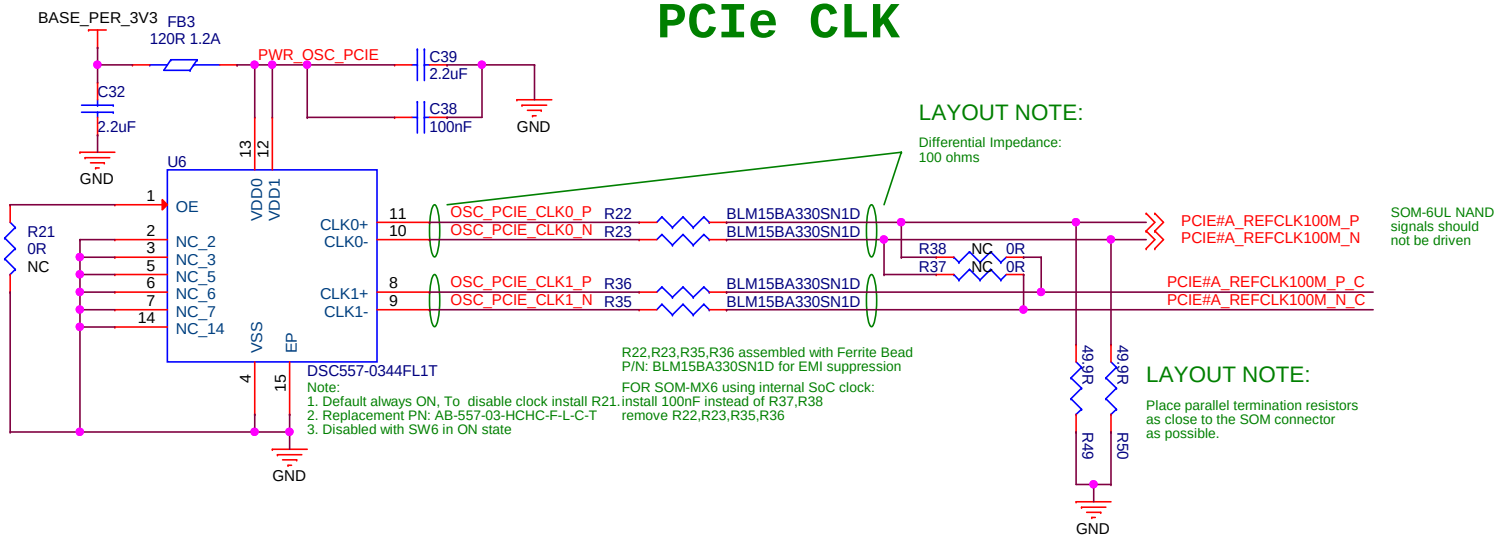


Variscite

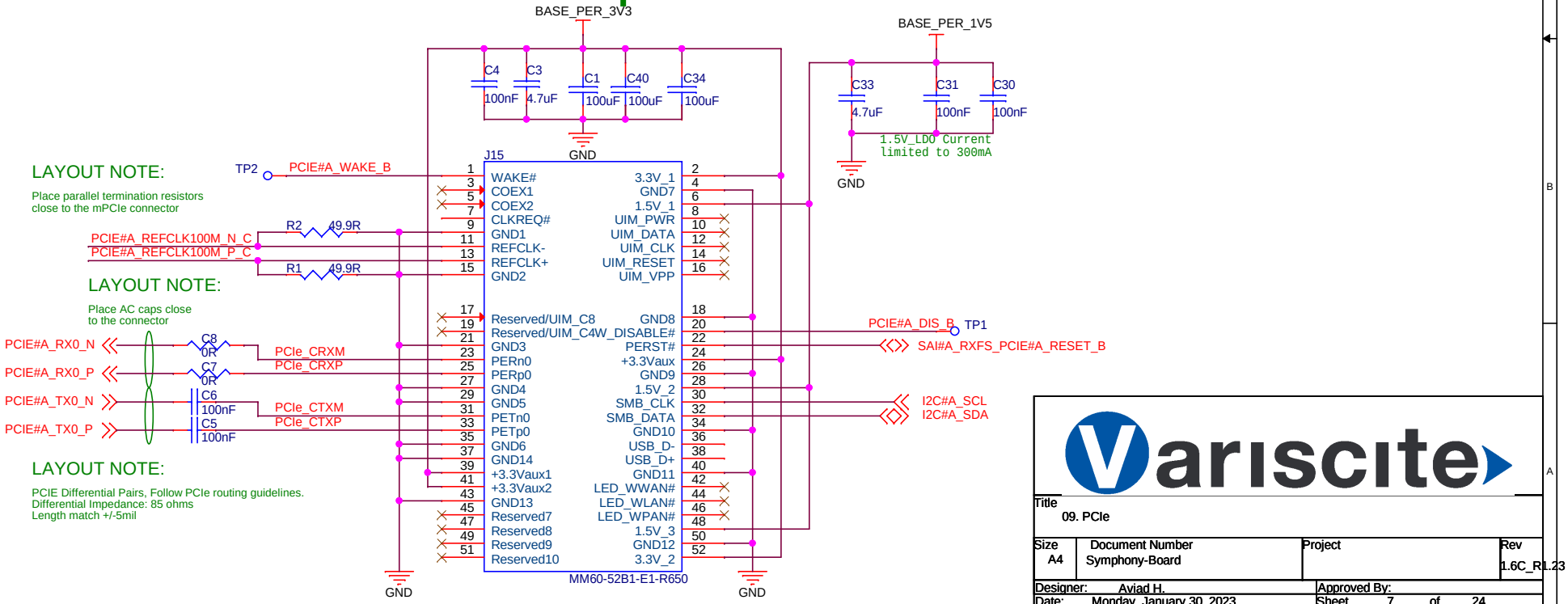
Title: 08. Ethernet			
Size: A3	Document Number: Symphony-Board	Project: Symphony-Board	Rev: 1.6C_R1.23
Designer: Aviad H.		Approved By:	
Date: Monday, January 30, 2023		Sheet 6 of 24	

09. PCIe

PCIe CLK



mPCIexp

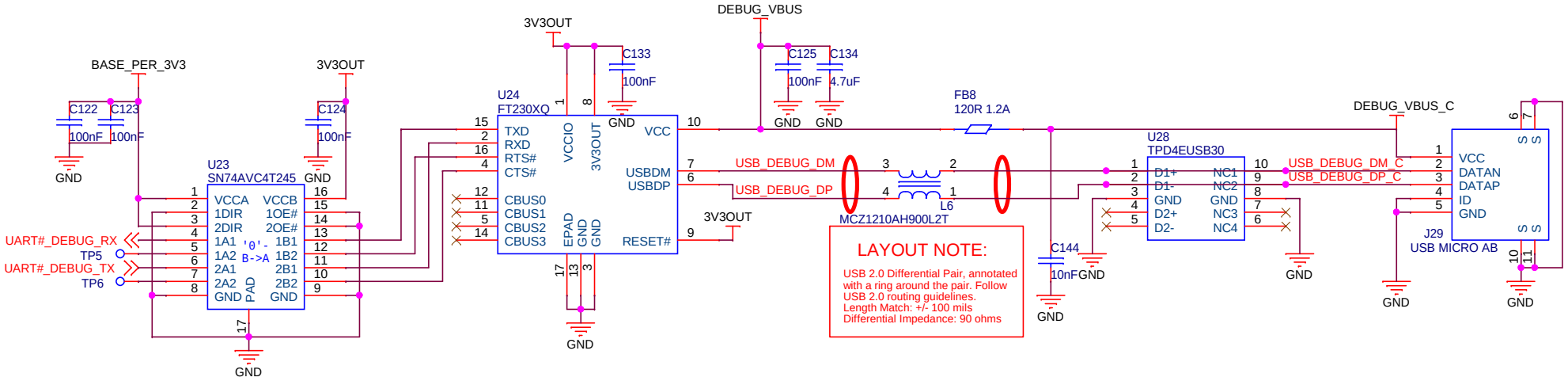


Variscite

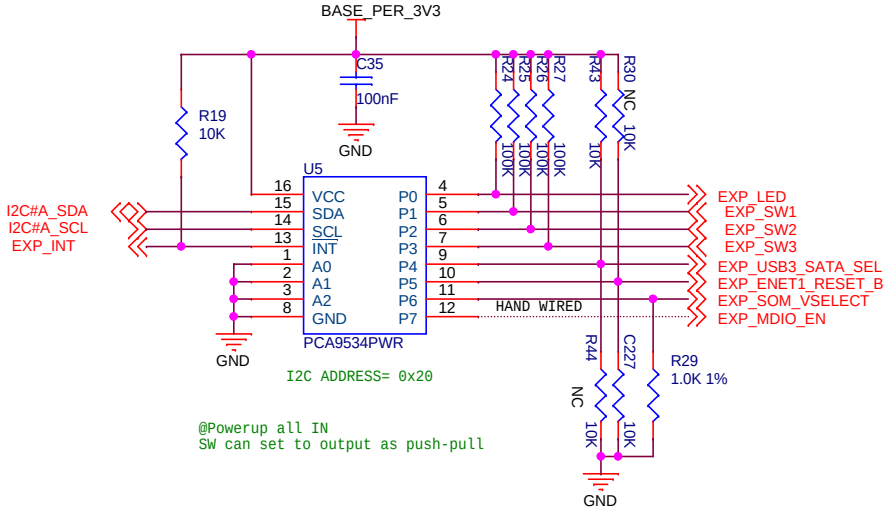
Title: 09. PCIe			
Size: A4	Document Number: Symphony-Board	Project:	Rev: 1.6C_R1.23
Designer: Aviad H.		Approved By:	
Date: Monday, January 30, 2023		Sheet 7 of 24	

10. Debug, GPIO Exp, Buttons, LED

USB UART DEBUG

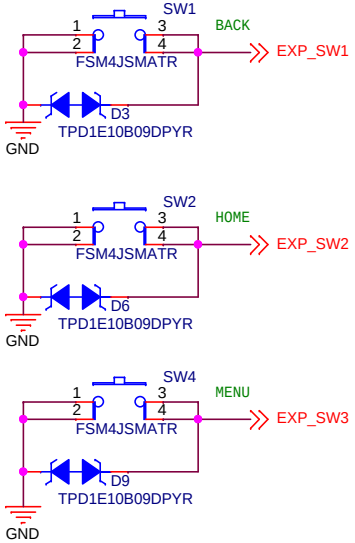


GPIO EXPANDER

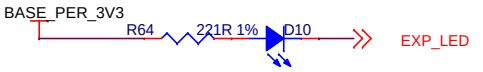


In VAR-SOM-MX8 SOM pin 29 EXP_INT is referenced to 1.8V.
When using pin 29 as an input pin driven by higher input voltage,
use an external voltage divider or limit the current using a series resistor to a maximum of 1mA.

GP BUTTON



GP LED

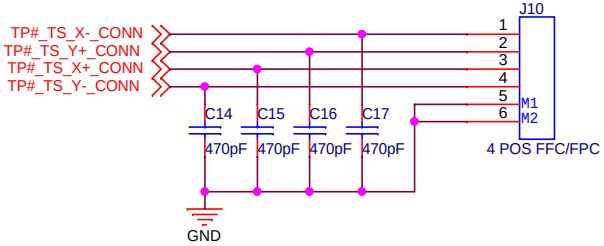


Variscite

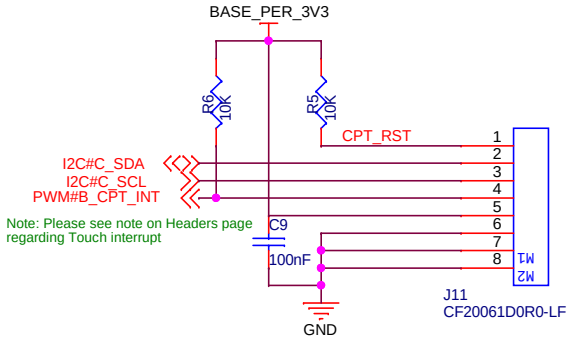
Title: 10. Debug, GPIO Exp, Buttons, LED			
Size: A4	Document Number: Symphony-Board	Project:	Rev: 1.6C_R1.23
Designer: Aviad H.		Approved By:	
Date: Monday, January 30, 2023		Sheet 8 of 24	

11. LVDS, DSI, Touch

RESISTIVE TOUCH

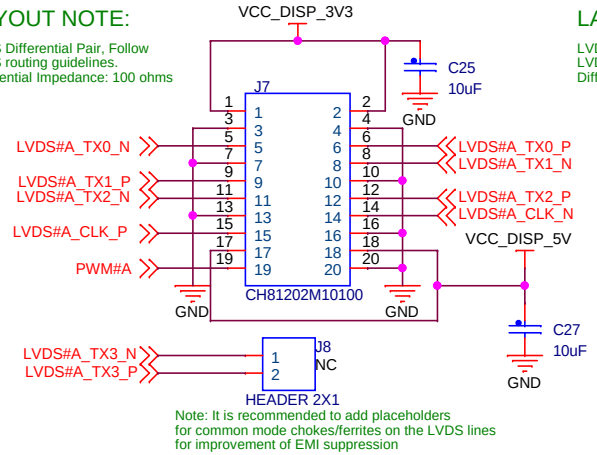


CAPACITIVE TOUCH



LVDS DISPLAY A

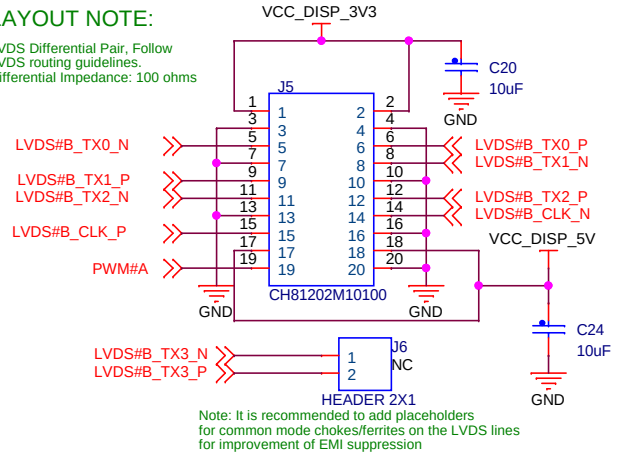
LAYOUT NOTE:
LVDS Differential Pair, Follow LVDS routing guidelines.
Differential Impedance: 100 ohms



Note: It is recommended to add placeholders for common mode chokes/ferrites on the LVDS lines for improvement of EMI suppression

LVDS DISPLAY B

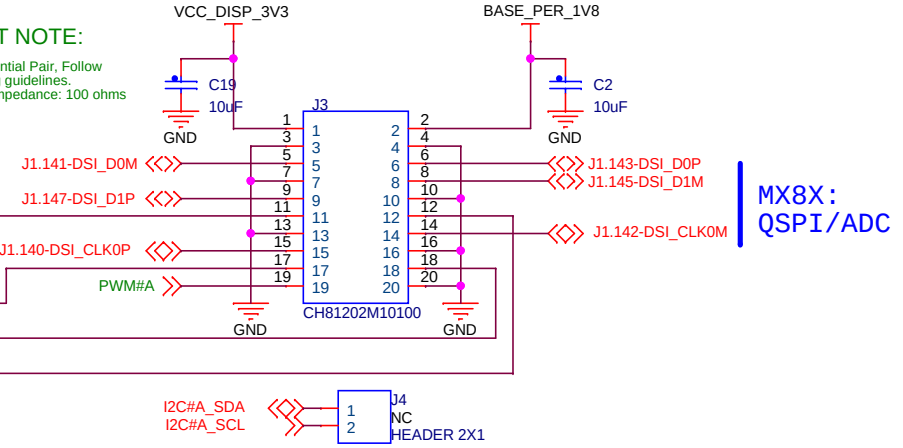
LAYOUT NOTE:
LVDS Differential Pair, Follow LVDS routing guidelines.
Differential Impedance: 100 ohms



Note: It is recommended to add placeholders for common mode chokes/ferrites on the LVDS lines for improvement of EMI suppression

MIPI DSI DISPLAY

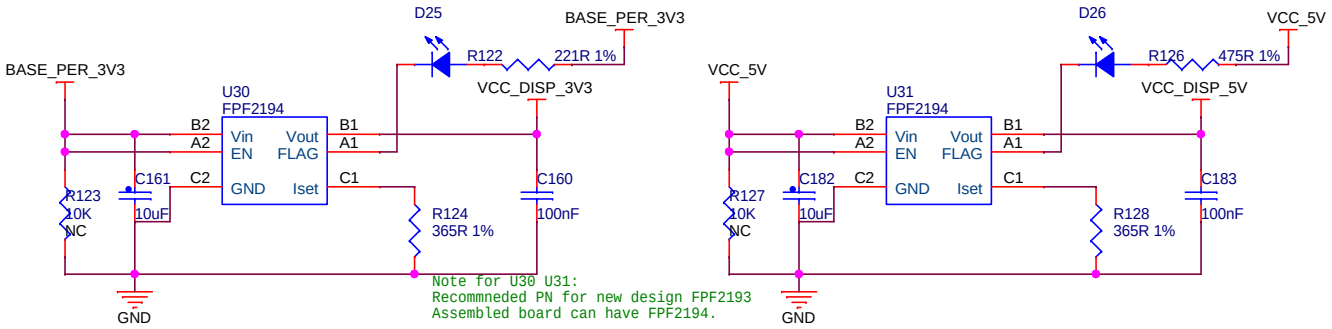
LAYOUT NOTE:
LVDS Differential Pair, Follow LVDS routing guidelines.
Differential Impedance: 100 ohms



See note in : "Headers" Page 14

J1.57_EXT
CB_WDOG_B
J1.82-USB#A_HOST_PWR
CB-USB#A_HOST_PWR

Short circuit protection



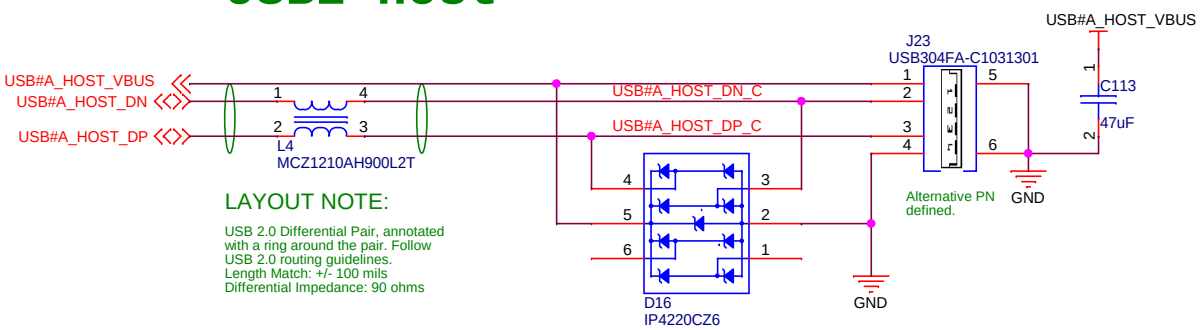
Note for U30 U31:
Recommneded PN for new design FPF2193
Assembled board can have FPF2194.

Variscite

Title: 11. LVDS, DSI, Touch			
Size: A4	Document Number: Symphony-Board	Project: Symphony-Board	Rev: 1.6C_R1.2
Designer: Aviad H.		Approved By:	
Date: Monday, January 30, 2023		Sheet 9 of 24	

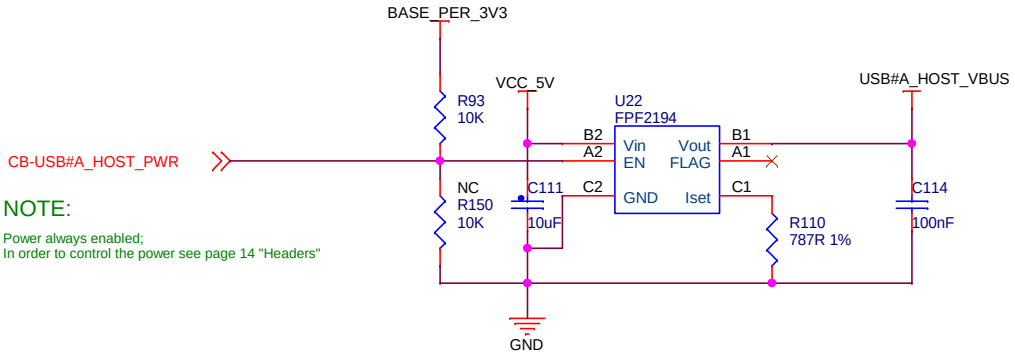
12. USB2 Host

USB2 Host



LAYOUT NOTE:

USB 2.0 Differential Pair, annotated with a ring around the pair. Follow USB 2.0 routing guidelines.
Length Match: +/- 100 mils
Differential Impedance: 90 ohms



NOTE:

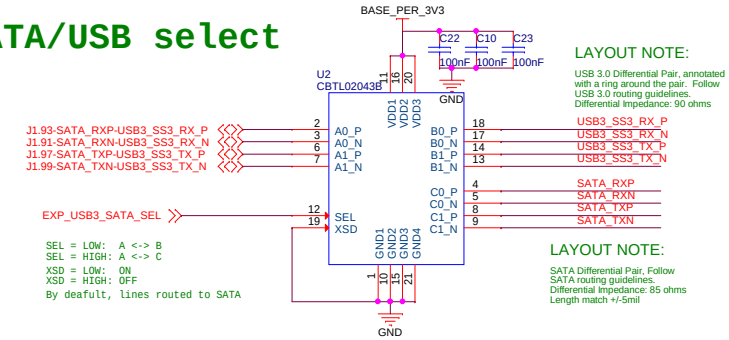
Power always enabled;
In order to control the power see page 14 "Headers"

Variscite

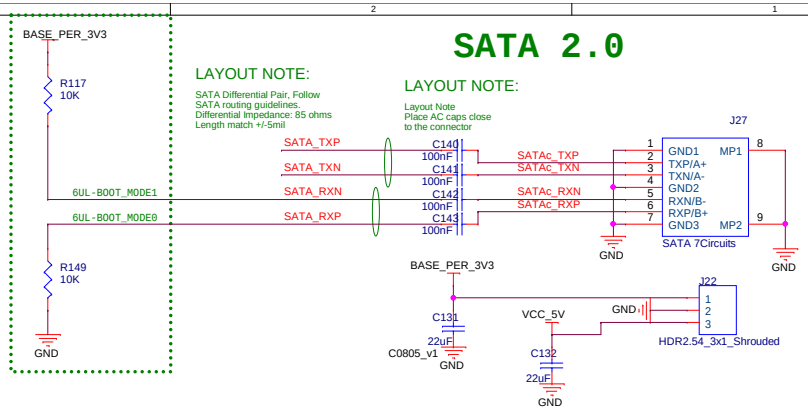
Title: 12. USB2 Host			
Size: A4	Document Number: Symphony-Board	Project: Symphony-Board	Rev: 1.6C_R1.2
Designer: Aviad H.		Approved By:	
Date: Monday, January 30, 2023		Sheet 10 of 24	

13. USB3, uSATA

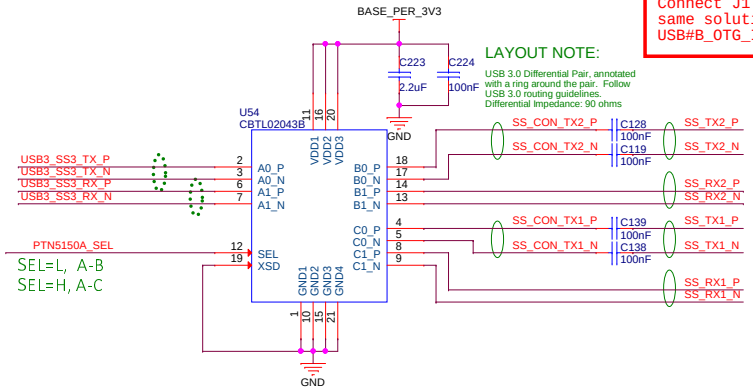
SATA/USB select



SATA 2.0

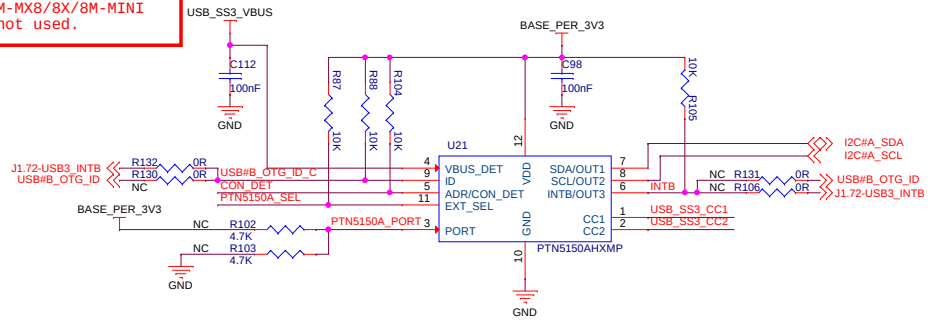


USB TYPE C Circuitry

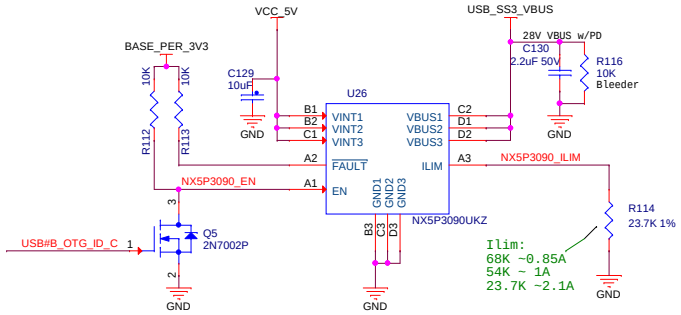


Usage of native USB_ID for iMX8MP requires patches not included in the formal release, pull up should be to 1.8V.
For simple OTG function for VAR-SOM-MX8M-PLUS Connect J1.72 GPIO to U22 PTN ID output - same solution appIies also for VAR-SOM-MX8/8X/8M-MINI USB#B_OTG_ID can be left floating if not used.

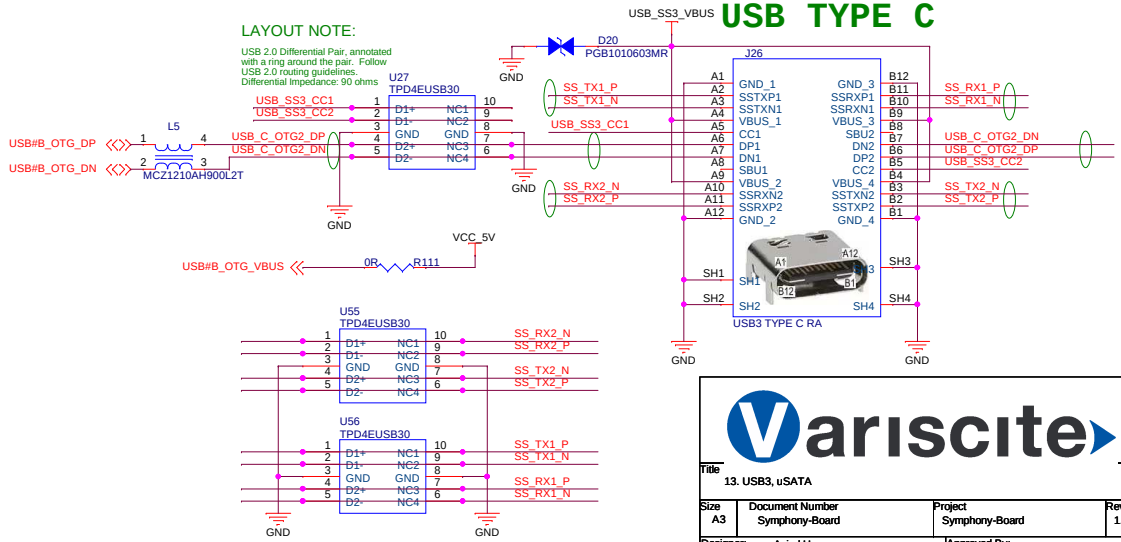
Config Channel Logic Detection & Indication of Plug Orientation



5V Source Load Switch



USB TYPE C

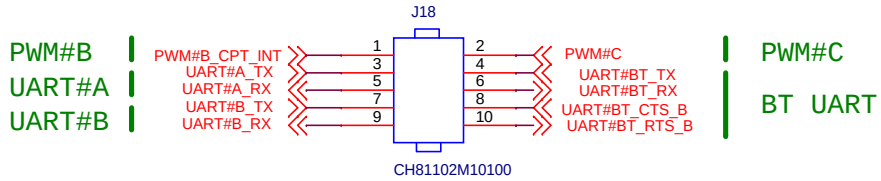


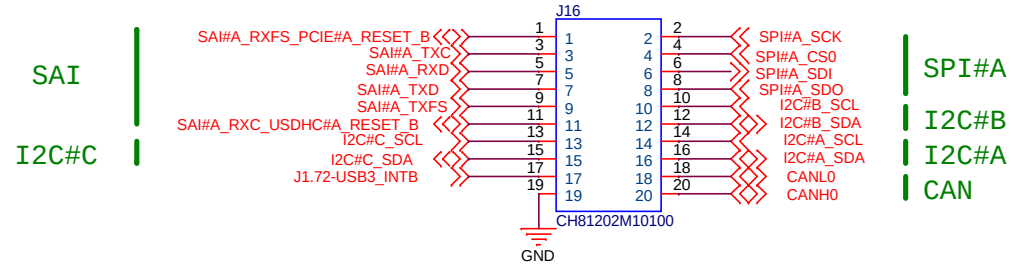
Variscite

Title: 13. USB3, uSATA			
Size: A3	Document Number: Symphony-Board	Project: Symphony-Board	Rev: 1.6C_R1.23
Designer: Aviad H.		Approved By:	
Date: Monday, January 30, 2023		Sheet 11 of 24	

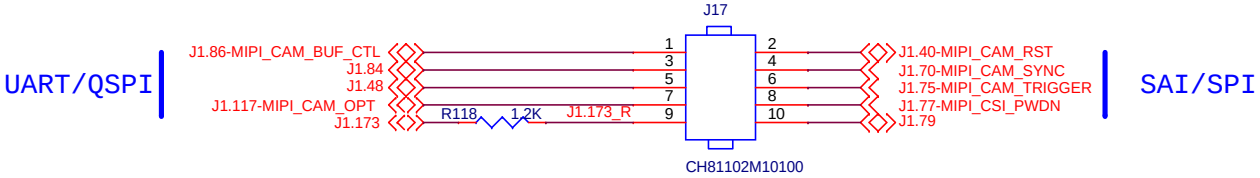
14. Headers

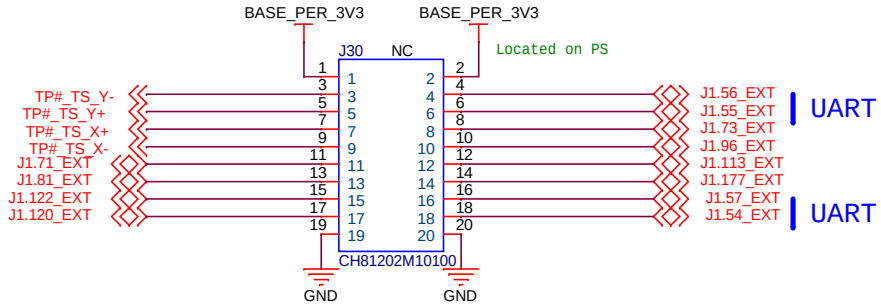
Headers arranged for compatible alternate function





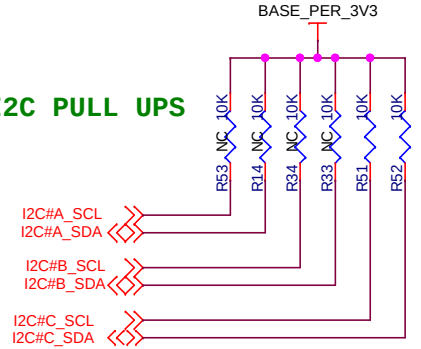
Headers arranged for partial compatible alternate function





For complete header alternate function refer to "VAR-SOMs_Compatibility_and_Pinout.XLS " located at: ftp://ftp.variscite.com/SOM_Compatibility

I2C PULL UPS



I2C_A has internal pulls in Camera buffer

I2C_B has internal pulls in MX6/MX8/MX8X/MX8MP SOMs.
For MX8MM/MX8MN/6UL SOMs - external pull ups should be added.

COLD RESET ON WDOG_B EVENT for MX6/SOLO and 6UL SOMs

Listed above SOMs require short on headers to get "reboot" to function.
For all other watch dog looped on SOM

CB_WDOG_B	Symphony Board reset circuitry watch dog input	See J3.17
J1.57_EXT	SOM_6UL: PIN57 WDOG1_B	See J3.11
PWM#B_CPT_INT	MX6/SOLO: PIN68 WDOG1_B	See J18.1

USB#A Host VBUS power control

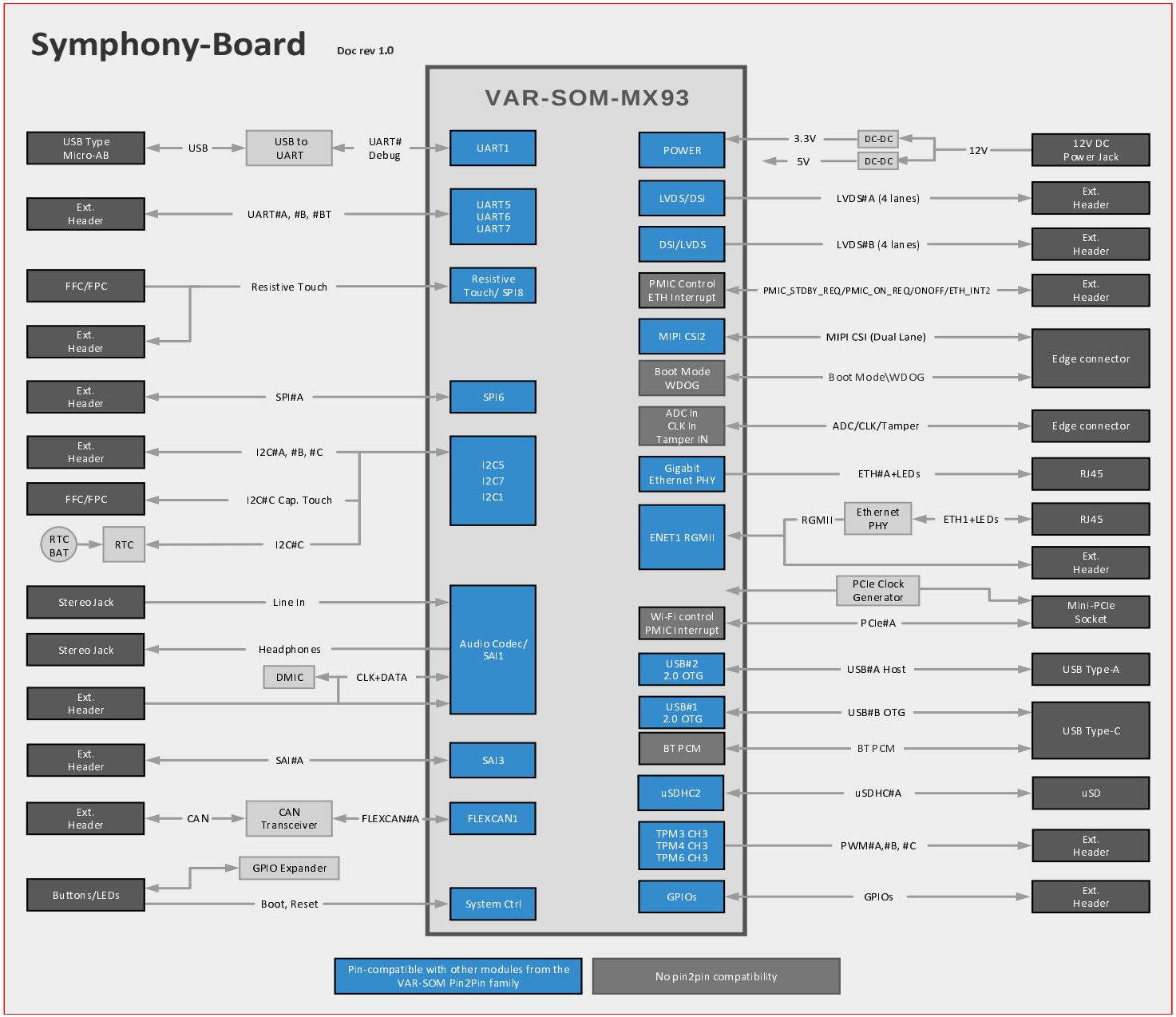
In order to control the USB#A HOST VBUS power a short is required:

CB-USB#A_HOST_PWR	Symphony Board U22 control input	See J3.12
J1.82-USB#A_HOST_PWR		See J3.18

Variscite

Title: 14. Headers			
Size: A4	Document Number: Symphony-Board	Project: Symphony-Board	Rev: 1.6C_R1.2
Designer: Aviad H.		Approved By:	
Date: Monday, January 30, 2023		Sheet 12 of 24	

02. Block Diagram VAR-SOM-MX93



Variscite

Title: 02. Block Diagram VAR-SOM-MX93			
Size: A3	Document Number: Symphony-Board	Project: Symphony-Board	Rev: 1.6C_R1.23
Designer: Aviad H.		Approved By:	
Date: Monday, January 30, 2023		Sheet 21 of 24	

04. VAR-SOM-MX93 Connector

		GND	2	GND			
ETHA_MDI_C_P	1.8V level signal on non EC		4	QOS.RGMII_RD3/I/FLEXIO2.FLEXIO19/GPIO4.IO19/*ETH0_MDI_C_P			
ETHA_MDI_C_M	1.8V level signal on non EC		6	QOS.RGMII_RD1/I/LPTMR2.ALT1/FLEXIO2.FLEXIO11/GPIO4.IO11/*ETH0_MDI_C_M			
		GND	8	GND			
ETHA_MDI_D_P	1.8V level signal on non EC		10	QOS.RGMII_RD2/I/LPTMR2.ALT2/FLEXIO2.FLEXIO12/GPIO4.IO12/*ETH0_MDI_D_P			
ETHA_MDI_D_M	1.8V level signal on non EC		12	QOS.RGMII_RD3/I/LPTMR2.ALT3/FLEXIO2.FLEXIO13/GPIO4.IO13/*ETH0_MDI_D_M			
		GND	14	GND			
ETHA_LED_LINK_1G_10G_100G	1.8V level signal on non EC		16	QOS.RGMII_RXC/QOS_RX_ER/I/FLEXIO2.FLEXIO9/GPIO4.IO9/*ETH0_LED_LINK			
ADI_DMIC_CLK			18	SAI1.TX_DATA0/UART2.RTS_B/SPI1.SCK/UART1.DTR_B/CAN1.TX/GPIO1.IO13/BOOT_MODE3/*DMIC_CLK			
ADI_DMIC_DATA			20	UART2.RX/UART1.CTS_B/SPI2.SOUT/TPM1.CH2/SAI1.MCLK/GPIO1.IO6/*DMIC_DATA			
SAIHA_RXC_USDHC4A_RESET_B			22	GPIO2.IO18/SAI3.RX_BCLK/I3.DSILCDIF.D14/SPI5.PCS0/SPI4.PCS0/TPM5.CH2/FLEXIO1.FLEXIO18			
SAIHA_TXFS			24	GPIO2.IO26/USDHC3.DATA2/PDM.BIT_STREAM1/LCDIF.D22/TPM5.CH0/DAP_TDI/SPI8.PCS1/SAI3.TX_SYNC			
SAIHA_TXD0			26	GPIO2.IO21/SAI3.TX_DATA0/PDM.CLK/LCDIF.D17/SPI5.SCK/SPI4.SCK/TPM4.CH1/SAI3.RX_BCLK			
		GND	28	GND			
J1.30-ENET_MDIO	Goes trought level translator		30	QOS.MDIO/I3C2.SDA/USB1.OTG_PWR/FLEXIO2.FLEXIO/GPIO4.IO1			
		VCC_SOM	32	VBAT			
		VCC_SOM	34	VBAT			
J1.36			36	NC1			
J1.38_POWER			38	NC1			
J1.40-MIPI_CAM_RST	1.8V level signal		40	NC2			
				CLKO2/I/FLEXIO1.FLEXIO27/GPIO3.IO27			
			42				
BOOT# SEL			44	BOOT_SEL			
FLEXCAN#A TX			46	PDM.CLK/MQS1.LEFT/I/LPTMR1.ALT1/GPIO1.IO8/CAN1.TX			
FLEXCAN#A RX			48	PDM.BIT_STREAM0/MQS1.RIGHT/SPI1.PCS1/TPM1.EXTCLK/LPTMR1.ALT2/GPIO1.IO9/CAN1.RX			
J1.48-I			50	GPIO2.IO30/SPI3.SOUT/I/SAI3.DI4.CDIF.D6/TPM4.EXTCLK/UART7.CTS_B/I2C8.SDA/FLEXIO1.FLEXIO10			
UART#BT_RTS_B	1.8V level signal. UART can be used if BT disabled. Has an internal 1K pull down		52	DAP.TMS_SWD/O/I/FLEXIO2.FLEXIO31/GPIO3.IO29/UART5.RTS_B			
UART#BT_TX	1.8V level signal. UART can be used if BT disabled		54	DAP.TDO_TRACESWO/MQS2.RIGHT/I/CAN2.RX/FLEXIO1.FLEXIO31/GPIO3.IO31/UART5.TX			
J1.54-ENET1_RGMII_RXD3	1.8V level signal		56	ENET2.RGMII_RD3/SPDIF1.OUT/SPDIF2.IN/MQS2.LEFT/FLEXIO2.FLEXIO27/GPIO4.IO27			
J1.56-ENET1_RGMII_TXD2	1.8V level signal		58	ENET2.RGMII_TD2/ENET2.TX_CLK/SAI2.RX_DATA1/I/FLEXIO2.FLEXIO17/GPIO4.IO17			
J1.58-I	1.8V level signal on non EC		60	QOS.RGMII_TXC/QOS_TX_ER/I/FLEXIO2.FLEXIO7/GPIO4.IO7/*INC			
USDHC#A_CLK	<Note>		62	USDHC2.CLK/QOS.1588_EVENT0_OUT/I/I3C2.SDA/I/FLEXIO1.FLEXIO1/GPIO3.IO1			
USDHC#A_DAT0	<Note>		64	USDHC2.DATA0/ENET2.1588_EVENT0_OUT/CAN2.TX/FLEXIO1.FLEXIO3/GPIO3.IO3			
USDHC#A_CMD	<Note>		66	USDHC2.CMD/ENET2.1588_EVENT0_IN/I3C2.PUR/I3C2.PUR_B/FLEXIO1.FLEXIO2/GPIO3.IO2			
		GND	68	GND			
PWM#B_CPT_INT			70	GPIO2.IO25/USDHC3.DATA1/CAN2.TX/LCDIF.D21/TPM4.CH3/DAP.TCLK_SWCLK/SPI7.PCS1/FLEXIO1.FLEXIO25			
J1.70-MIPI_CAM_SYNC			72	NC3			
J1.72-USB3_INT8			74	PDM.BIT_STREAM1/M33.NMI/SPI2.PCS1/TPM2.EXTCLK/LPTMR1.ALT3/GPIO1.IO10			
J1.74-ENET_MDC	Goes trought level translator		76	QOS.MDC/I3C2.SCL/USB1.OTG_ID/FLEXIO2.FLEXIO0/GPIO4.IO0			
		GND	78	GND			
		GND	80	GND			
USDHC#A_CD_B	<Note>		82	USDHC2.CD_B/QOS.1588_EVENT0_IN/I3C2.SCL/I/FLEXIO1.FLEXIO0/GPIO3.IO0			
J1.82-USB#A_HOST_PWR	1.8V level signal on special assembly SOM		84	NC5			
J1.84-I			86	USDHC3.DATA0/I/FLEXSPI.A_DATA0/I/FLEXIO1.FLEXIO22/GPIO3.IO22/*INC			
J1.86-MIPI_CAM_BUF_CTL			88	GPIO2.IO17/SAI3.MCLK/I3.DI8.LCDIF.D13/UART3.RTS_B/SPI4.PCS1/UART4.RTS_B/FLEXIO1.FLEXIO17			
I2C#A_SCL			90	GPIO2.IO23/USDHC3.CMD/SPDIF1.OUT/LCDIF.D19/TPM6.CH1/I2C5.SCL/FLEXIO1.FLEXIO23			
I2C#C_SDA			92	I2C1.SDA/I3C1.SDA/UART1.RIN_B/TPM2.CH0/GPIO1.IO1			
I2C#C_SCL			94	I2C1.SCL/I3C1.SCL/UART1.DCB_B/TPM2.CH0/GPIO1.IO0			
USB#B_OTG_ID	<Note>		96	USB1_ID			
J1.96-ENET1_RGMII_TXC	1.8V level signal		98	ENET2.RGMII_TXC/ENET2.TX_ER/SAI2.TX_BCLK/FLEXIO2.FLEXIO21/GPIO4.IO21			
POR_B#_3V3	3.3V level signal. Open drain. Has an internal 100k pull up to 1.8V		100	SYS_NRST			
PCIE#A_REFCLK100M_N			102	NC6			
PCIE#A_REFCLK100M_P			104	NC7			
USB#A_HOST_VBUS	5V level		106	USB2_VBUS			
USB#B_OTG_VBUS	5V level		108	USB1_VBUS			
USB#A_HOST_DN			110	USB2_D_N			
USB#A_HOST_DP			112	USB2_D_P			
		GND	114	GND			
USB#B_OTG_DN			116	USB1_D_N			
USB#B_OTG_DP			118	USB1_D_P			
		GND	120	GND			
J1.120-ENET1_RGMII_RX_CTL	1.8V level signal		122	ENET2.RGMII_RX_CTL/UART4.DSR_B/SAI2.TX_DATA0/I/FLEXIO2.FLEXIO22/GPIO4.IO22			
J1.122-ENET1_RGMII_RXC	1.8V level signal		124	ENET2.RGMII_RD0/UART4.RX/SAI2.TX_DATA2/FLEXIO2.FLEXIO24/GPIO4.IO24			
UART#A_TX			126	GPIO2.IO8/SPI3.PCS0/ISI.D2/LCDIF.D4/TPM6.CH0/UART7.TX/I2C7.SDA/FLEXIO1.FLEXIO8			
		GND	128	GND			
PCIE#A_TX0_N	1.8V level signal		130	WIFI_HOST_WAKE			
PCIE#A_TX0_P	1.8V level signal		132	BT_CEV_WAKE			
		GND	134	GND			
PCIE#A_RX0_P	1.8V level signal		136	BT_HOST_WAKE			
PCIE#A_RX0_N	1.8V level signal. No internal pull-up		138	PMIC_NINT			
		GND	140	GND			
J1.140-DSI_CLK0P	1.8V level signal. Has an internal 1k Pull down		142	PMIC_STBY_REQ			
J1.142-DSI_CLK0M	1.8V level signal. Has an internal 1k Pull down		144	PMIC_ON_REQ			
		GND	146	GND			
J1.146-HDMI_D1P	1.8V level signal		148	ADC_IN0			
J1.148-HDMI_D1M	1.8V level signal		150	ADC_IN1			
J1.150-HDMI_CLKM	1.8V level signal		152	ADC_IN2			
J1.152-HDMI_CLKP	1.8V level signal. Has an internal 1k Pull down		154	CLK/RUESD_DIODE			
J1.154-HDMI_HPD	1.8V level signal		156	TAMPER0			
J1.156-I	1.8V level signal		158	TAMPER1			
		GND	160	GND			
LVDS#A_TX1_N			162	LVDS_D1_N/*DSI_D1_N			
LVDS#A_TX1_P			164	LVDS_D1_P/*DSI_D1_P			
LVDS#A_TX2_N			166	LVDS_D2_N/*DSI_D2_N			
LVDS#A_TX2_P			168	LVDS_D2_P/*DSI_D2_P			
LVDS#A_CLK_N			170	LVDS_CLK_N/*DSI_CLK_N			
LVDS#A_CLK_P			172	LVDS_CLK_P/*DSI_CLK_P			
		GND	174	GND			
I2C#B_SCL			176	GPIO2.IO7/SPI3.PCS1/ISI.D1/LCDIF.D3/SPI7.SCK/UART6.RTS_B/I2C7.SCL/FLEXIO1.FLEXIO7			
I2C#B_SDA			178	GPIO2.IO6/TPM5.CH0/PDM.BIT_STREAM1/LCDIF.D2/SPI7.SOUT/UART6.CTS_B/I2C7.SDA/FLEXIO1.FLEXIO6			
		GND	180	GND			
LVDS#B_CLK_N			182	DSI_CLK_N/*LVDS_CLK_N			
LVDS#B_CLK_P			184	DSI_CLK_P/*LVDS_CLK_P			
LVDS#B_TX0_N			186	DSI_D0_N/*LVDS_D0_N			
LVDS#B_TX0_P			188	DSI_D0_P/*LVDS_D0_P			
LVDS#B_TX1_N			190	DSI_D1_N/*LVDS_D1_N			
LVDS#B_TX1_P			192	DSI_D1_P/*LVDS_D1_P			
LVDS#B_TX2_N			194	DSI_D2_N/*LVDS_D2_N			
LVDS#B_TX2_P			196	DSI_D2_P/*LVDS_D2_P			
ACH_HPOUTFB			198	I2C2.SCL/I3C1.PUR/UART2.DCB_B/TPM2.CH2/SAI1.RX_SYNC/GPIO1.IO2/I3C1.PUR_B/*HPOUTFB			
ACH_HPLOUT			200	SAI1.RX_DATA0/SAI1.MCLK/SPI1.SCK/UART2.DSR_B/MQS1.RIGHT/GPIO1.IO14/*HPLOUT			
ACH_HPROUT				SAI1.TX_BCLK/UART2.CTS_B/SPI1.SIN/UART1.DSR_B/CAN1.RX/GPIO1.IO12/*HPROUT			

			1	QOS.RGMII_TX_CTL/I/FLEXIO2.FLEXIO6/GPIO4.IO6/*INC			
			3	QOS.RGMII_TD3/I/CAN2.TX/USB2.OTG_IDF/LEXIO2.FLEXIO3/GPIO4.IO3/*ETH0_MDI_A_P			
			5	QOS.RGMII_TD2/QOS.TX_CLK/CAN2.RX/USB2.OTG_OC/FLEXIO2.FLEXIO5/GPIO4.IO3/*ETH0_MDI_A_M			
		GND	7	GND			
			9	QOS.RGMII_TD1/I3C2.PUR/USB1.OTG_OC/FLEXIO2.FLEXIO4/GPIO4.IO4/I3C2.PUR_B/*ETH0_MDI_B_P			
			11	QOS.RGMII_TD0/I/FLEXIO2.FLEXIO5/GPIO4.IO5/*ETH0_MDI_B_M			
		GND	13	GND			
			15	QOS.RGMII_RX_CTL/I/USB2.OTG_PWR/FLEXIO2.FLEXIO8/GPIO4.IO8/*ETH0_LED_ACT			
			17	GPIO2.IO24/USDHC3.DATA0/LCDIF.D20/TPM3.CH0/BAP TDO_TRACESWO/SPI6.PCS1/FLEXIO1.FLEXIO24			
		GND	19	GND			
			21	GPIO2.IO20/SAI3.RX_DATA0/PDM.BIT_STREAM0/LCDIF.D16/SPI5.SOUT/SPI4.SOUT/TPM3.CH1/FLEXIO1.FLEXIO20			
			23	GPIO2.IO19/SAI3.RX_SYNC/PDM.BIT_STREAM3/LCDIF.D15/SPI5.SIN/SPI4.SIN/TPM5.CH2/SAI3.TX_DATA0			
			25	GPIO2.IO16/SAI3.TX_BCLK/PDM.BIT_STREAM0/LCDIF.D12/UART3.CTS_B/SPI4.PCS2/UART4.CTS_B/FLEXIO1.FLEXIO16			
		GND	27	GND			
			29	CLKO1/I/FLEXIO1.FLEXIO26/GPIO3.IO26			
			31	USDHC3.DATA1/FLEXSPI.A_DATA1/I/FLEXIO1.FLEXIO23/GPIO3.IO23/*INC			
			33	USDHC3.DATA2/FLEXSPI.A_DATA2/I/FLEXIO1.FLEXIO24/GPIO3.IO24/*INC			
			35	USDHC3.DATA3/FLEXSPI.A_DATA3/I/FLEXIO1.FLEXIO25/GPIO3.IO25/*INC			
		GND	37	GND			
			39	GPIO2.IO0/I2C3.SDA/ISI.PCLK/LCDIF.PCLK/SPI6.PCS0/UART5.TX/I2C5.SDA/FLEXIO1.FLEXIO0			
			41				
			43	GPIO2.IO1/I2C3.SCL/ISI.D0/LCDIF.DE/SPI6.SIN/UART5.RX/I2C5.SCL/FLEXIO1.FLEXIO1			
			45	GPIO2.IO3/I2C4.SCL/ISI.LINE_VAL/D/LCDIF.HSYNC/SPI6.SCK/UART5.RTS_B/I2C6.SCL/FLEXIO1.FLEXIO3			
			47	GPIO2.IO2/I2C4.SDA/ISI.FRAME_VAL/D/LCDIF.VSYNC/SPI6.SOUT/UART5.CTS_B/I2C6.SDA/FLEXIO1.FLEXIO2			
		GND	49	GND			
			51				SOM_3V3
			53	DAP.TCLK_SWCLK/I/FLEXIO1.FLEXIO30/GPIO3.IO30/UART5.CTS_B			
			55	DAP.TDI/MQS2.LEFT/I/CAN2.TX/FLEXIO2.FLEXIO30/GPIO3.IO28/UART5.RX			
			57	ENET2.RGMII_TD3/ISA2.RX_DATA0/I/FLEXIO2.FLEXIO16/GPIO4.IO16			
			59	ENET2.RGMII_RXC/ENET2.RX_ER/ISA2.TX_DATA1/I/FLEXIO2.FLEXIO23/GPIO4.IO23			
		GND	61	GND			
			63	USDHC2.DATA2/ENET2.1588_EVENT1_OUT/MQS2.RIGHT/I/FLEXIO1.FLEXIO5/GPIO3.IO5			
			65	USDHC2.DATA1/ENET2.1588_EVENT1_IN/CAN2.RX/I/FLEXIO1.FLEXIO4/GPIO3.IO4			
			67	USDHC2.DATA3/LPTMR2.ALT1/MQS2.LEFT/I/FLEXIO1.FLEXIO6/GPIO3.IO6			
		GND	69	GND			
			71	GPIO2.IO27/USDHC3.DATA3/CAN2.RX/LCDIF.D23/TPM6.CH3/DAP.TMS_SWDIO/SPI5.PCS1/FLEXIO1.FLEXIO27			
			73	ENET2.RGMII_RD2/UART4.CTS_B/SAI2.MCLK/MQS2.RIGHT/I/FLEXIO2.FLEXIO26/GPIO4.IO26			
			75	ENET2.RGMII_TD0/UART4.TX/SAI2.RX_DATA3/I/FLEXIO2.FLEXIO19/GPIO4.IO19			
			77	CLKO3/I/FLEXIO2.FLEXIO28/GPIO4.IO28			
			79	GPIO2.IO1/SPI3.SCK/ISI.DS/LCDIF.D7/TPM5.EXTCLK/UART7.RTS_B/I2C8.SCL/FLEXIO1.FLEXIO11			
			81	NC4			
			83	ENET2.RGMII_RD1/SPDIF1.IN/SAI2.TX_DATA3/I/FLEXIO2.FLEXIO25/GPIO4.IO25			
			85	UART1.RX/SECO.RX/SPI2.SIN/TPM1.CH0/GPIO1.IO4			
			87	UART1.TX/SECO.TX/SPI2.PCS0/TPM1.CH1/GPIO1.IO5/BOOT_MODE0			
			89	GPIO2.IO22/USDHC3.CLK/SPDIF1.IN/LCDIF.D18/TPM5.CH1/TPM6.EXTCLK/I2C5.SDA/FLEXIO1.FLEXIO22			
		GND	91	GND			
			93	BT_PCM_CLK			
			95	BT_PCM_IN			
		GND	97	GND			
			99	BT_PCM_OUT			
			101	BT_PCM_SYNC			
		GND	103	GND			
		VCC_SOM	105	VBAT			
		VCC_SOM	107	VBAT			
		VCC_SOM	109	VBAT			
		VCC_SOM	111	VBAT			
		VCC_SOM	113	VBAT	1.8V level signal		
				ENET2.RGMII_TX_CTL/UART4.DTR_B/SAI2.TX_SYNC/I/FLEXIO2.FLEXIO20/GPIO4.IO20			
				GPIO2.IO5/TPM4.CH0/PDM.BIT_STREAM0/LCDIF.D1/SPI7.SIN/UART6.RX/I2C6.SCL/FLEXIO1.FLEXIO5			
				NC8			
				MIPI_CSI1_D0_P			
				MIPI_CSI1_D0_N			
				MIPI_CSI1_D1_N			
				MIPI_CSI1_D1_P			
				NC9			
				NC10			
				WDOG1.WDOG_ANY/I/I/GPIO1.IO15			
				NC11			
				MIPI_CSI1_CLK_P			
				MIPI_CSI1_CLK_N			
		GND		GND			
				ETH_INT_N/B			
				ON/OFF			
				USDHC3.CLK/FLEXSPI.A_SCLK/I/FLEXIO1.FLEXIO20/GPIO3.IO20/*INC			
				USDHC3.CMD/FLEXSPI.A_SS0_B/I/FLEXIO1.FLEXIO21/GPIO3.IO21/*INC			
		GND		GND			
				ADC_IN3			
				CLKIN2/ATX			
				NC12			
				NC13			
		GND		GND			
				LVDS_D0_N/*DSI_D0_N			
				LVDS_D0_P/*DSI_D0_P			
				LVDS_D3_N/*DSI_D3_N			
				LVDS_D3_P/*DSI_D3_P			
		GND		GND			
				GPIO2.IO4/TPM3.CH0/PDM.CLK/LCDIF.D0/SPI7.PCS0/UART6.TX/I2C6.SDA/FLEXIO1.FLEXIO4			
				NC14			
				GPIO2.IO9/SPI3.SIN/ISI.D3/LCDIF.D5/TPM3.EXTCLK/UART7.RX/I2C7.SCL/FLEXIO1.FLEXIO9			
				ENET2.RGMII_TD1/UART4.RTS_B/SAI2.RX_DATA2/I/FLEXIO2.FLEXIO18/GPIO4.IO18			
		GND		GND			
				DSI_D3_P/*LVDS_D3_P			
				DSI_D3_N/*LVDS_D3_N			
		GND		GND			
				GPIO2.IO14/UART3.TX/ISI.D6/LCDIF.D10/SPI8.SOUT/UART8.CTS_B/UART4.TX/FLEXIO1.FLEXIO14/*TS_X-			
				GPIO2.IO15/UART3.RX/ISI.D7/LCDIF.D11/SPI8.SCK/UART8.RTS_B/UART4.RX/FLEXIO1.FLEXIO15/*TS_X+			
				GPIO2.IO13/TPM4.CH2/PDM.BIT_STREAM0/LCDIF.D8/SPI8.PCS0/UART8.TX/I2C8.SDA/SAI3.RX_SYNC/*TS_Y+			
				GPIO2.IO12/TPM4.CH2/PDM.BIT_STREAM0/LCDIF.D9/SPI8.SIN/UART8.RX/I2C8.SCL/FLEXIO1.FLEXIO13/*TS_Y-			
				AGND			
				I2C2.SDA/I/UART2.RIN_B/TPM2.CH3/SAI1.RX_BCLK/GPIO1.IO3/*LINEIN1_LP			
				SAI1.TX_SYNC/SAI1.TX_DATA1/SPI1.PCS0/UART2.DTR_B/MQS1.LEFT/GPIO1.IO11/BOOT_MODE2/*LINEIN1_RP			

			1		1.8V level signal on non EC		J1.1
			3		1.8V level signal on non EC		ETH#A_MDI_A_P
			5		1.8V level signal on non EC		ETH#A_MDI_A_M
		GND	7		GND		
			9		1.8V level signal on non EC		ETH#A_MDI_B_P
			11		1.8V level signal on non EC		ETH#A_MDI_B_M
		GND	13		GND		
			15		1.8V level signal on non EC		ETH#A_LED_ACT
			17				PWM#A
		GND	19		GND		
			21				SAIHA_RXD
			23				SAIHA_RXFS_PCIE#A_RESET_B
			25				SAIHA_TXC
		GND	27		GND		
			29		1.8V level signal. Has an internal 12K pull down		EXP_INT
			31		1.8V level signal on special assembly SOM		J.31_33_35_PWR
			33		1.8V level signal on special assembly SOM		J.31_33_35_PWR
			35		1.8V level signal on special assembly SOM		J.31_33_35_PWR
		GND	37		GND		
			39		Cannot be configured as I2C3		SPI#A_CS0
			41		Cannot be configured as I2C3		
			43				SPI#A_SDI
			45				SPI#A_SCK
			47				SPI#A_SDO
		GND	49		GND		
			51		1.8V level signal. UART can be used if BT disabled		SOM_3V3
			53		1.8V level signal. UART can be used if BT disabled		UART#BT_CTS_B
			55		1.8V level signal		UART#BT_RX
			57		1.8V level signal		J1.55-ENET1_RGMII_TXD3
			59				J1.57-ENET1_RGMII_RXC
		GND	61		GND		
			63		<Note>		USDH#A_DAT2
			65		<Note>		USDH#A_DAT1
			67		<Note>		USDH#A_DAT3
		GND	69		GND		
			71		1.8V level signal		PWM#C
			73		1.8V level signal		J1.71-ENET1_RGMII_RXD2
			75		1.8V level signal		J1.73-ENET1_RGMII_TXD0
			77				J1.75-MIPI_CAM_TRIGGER
			79				J1.77-MIPI_CSI_PWDN
			81		NC4		J1.79
			83		1.8V level signal		J1.81-ENET1_RGMII_RXD1
			85				UART1_DEBUG_RX
			87				UART1_DEBUG_TX
			89				I2C#A_SDA
		GND	91		GND		
			93		1.8V level signal		J1.91-SATA_RXN-USB3_SS3_RX_N
			95		1.8V level signal		J1.93-SATA_RXP-USB3_SS3_RX_P
		GND	97		GND		
			99		1.8V level signal		J1.97-SATA_TXP-USB3_SS3_TX_P
			101		1.8V level signal		J1.99-SATA_TXN-USB3_SS3_TX_N
		GND	103		GND		
		VCC_SOM	105		VCC_SOM		
		VCC_SOM	107		VCC_SOM		
		VCC_SOM	109		VCC_SOM		
		VCC_SOM	111		VCC_SOM		
		VCC_SOM	113		VCC_SOM	1.8V level signal	
							J1.113-ENET1_RGMII_TX_CTL
							UART#B_RX
							J1.117-MIPI_CAM_OPT
							MIPI_CSI#A_DATA0_P
							MIPI_CSI#A_DATA0_N
							MIPI_CSI#A_DATA1_N
							MIPI_CSI#A_DATA1_P
							MIPI_CSI#A_DATA2_P
							MIPI_CSI#A_DATA2_N
							MIPI_CSI#A_DATA3_N
							MIPI_CSI#A_DATA3_P
							MIPI_CSI#A_CLK_P
							MIPI_CSI#A_CLK_N
		GND			GND		
							J1.141-DSI_D0M
					<Note>		J1.143-DSI_D0P
					1.8V level signal on special assembly SOM		J1.145-DSI_D1M
					1.8V level signal on special assembly SOM		J1.147-DSI_D1P
		GND			GND		
					1.8V level signal		
					1.8V level signal. Has an internal 1k Pull down		J1.151-HDMI_D2P
							J1.153-HDMI_D2M
							J1.155-HDMI_D0P
							J1.157-HDMI_D0M
		GND			GND		
							LVDS#A_TX0_N
							LVDS#A_TX0_P
							LVDS#A_TX3_N
							LVDS#A_TX3_P
		GND			GND		
							UART#B_TX
							J1.173
							UART#A_RX
					1.8V level signal		J1.177-ENET1_RGMII_TXD1
		GND			GND		
							LVDS#B_TX3_P
							LVDS#B_TX3_N
		GND			GND		
							TP#_TS_X-
							TP#_TS_X+
							TP#_TS_Y+
							TP#_TS_Y-
							ACH_AGND
							ACH_LINEIN_LP
							ACH_LINEIN_RP

Variscite

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Size: Custom	Document Number: Symphony-Board	Project: Symphony-Board	Rev: 1.0C_R2.23
Designer:	Author:	Approved By:	
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